Klystron 2 & 5 non-linearities measurement and linearisation method tests

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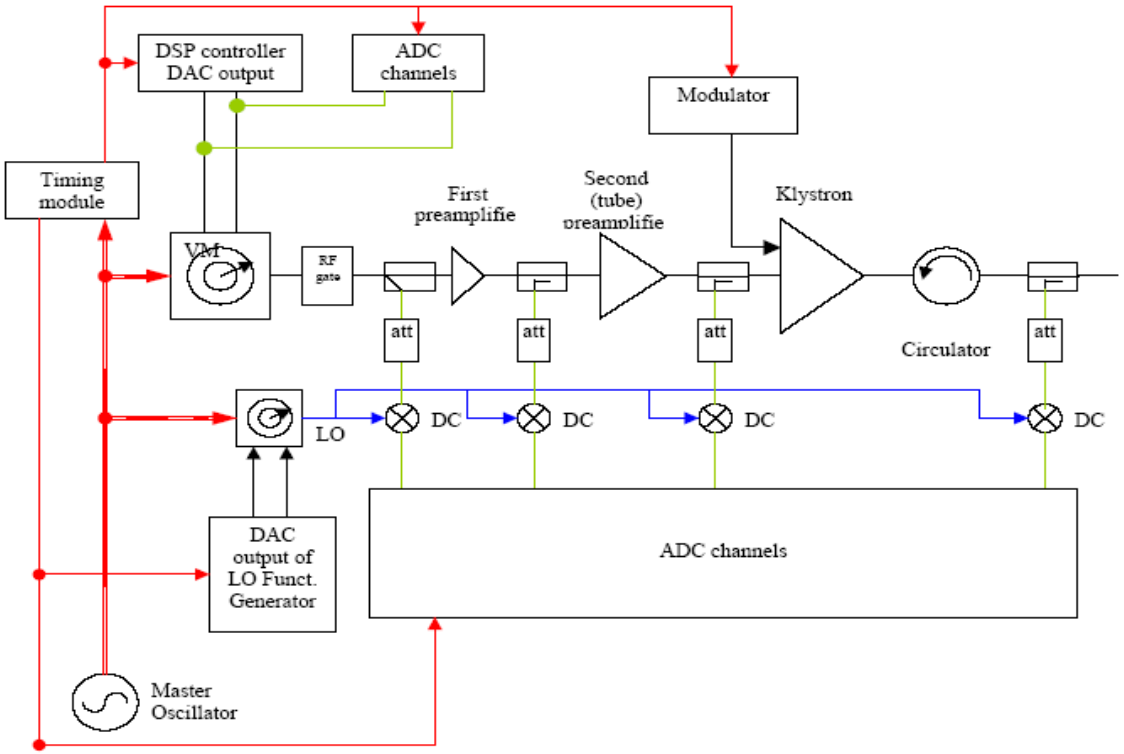
Outline

- Klystron 2 & 5 non-linearities measurements and results example,
- Linearisation algorithm principles,
- Klystron 5 linearisation (Simcon FPGA and DSP controller)
- Klystron 2 linearisation (Simcon FPGA controller)
- Conclusions
- Plans

Non-linearities measurement purpose

Goal:

To provide high power chain components characterization for the different working parameters.



This characterization will be used in the linearization method designing for a klystron and high power amplifiers.

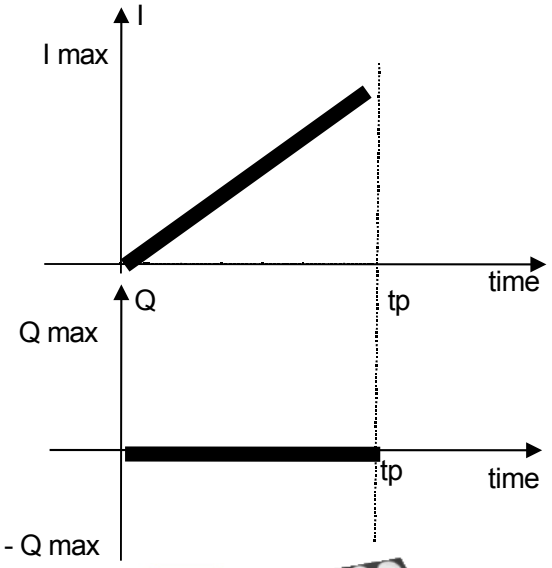
Thanks to provided diagnostic, one can also detect following anomalies:

- different HPC component malfunction,
- components saturations,
- phase or frequency offsets, etc.

High power chain non-linearities

Non-linearities and saturation phenomena:
-increasing the driving power -> non-linear amplifier behaviour
-constant increasing of driving power -> saturation
-different saturation level for a different working parameters values

Test signal (as far as nonlinearities are only amplitude dependent):
Signal parameters:
Pulse length – 1200 us,
Number of steps – 50 stp,
Signal range – 0 up to max. available level



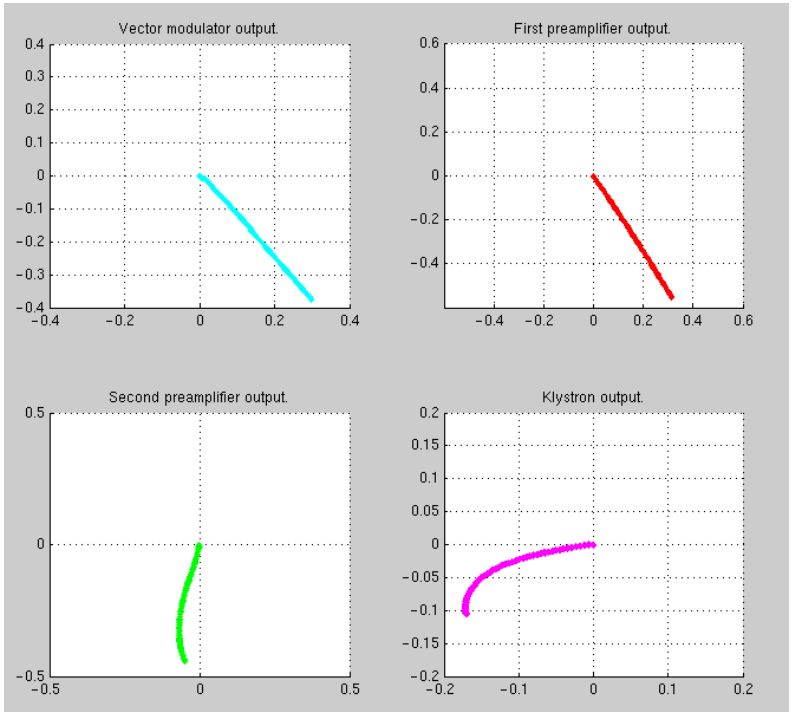
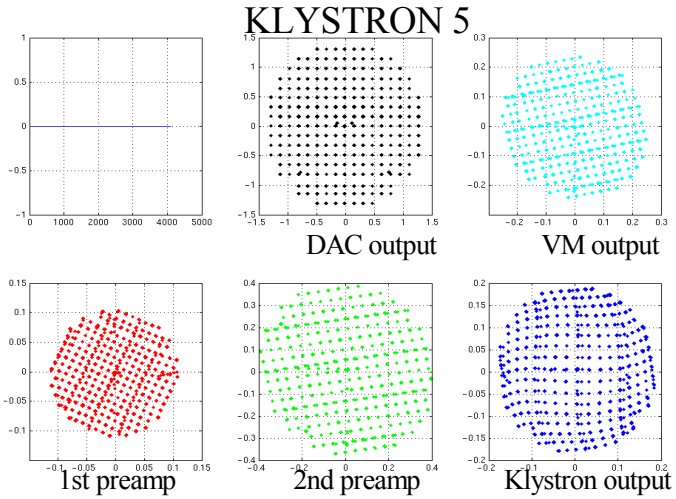
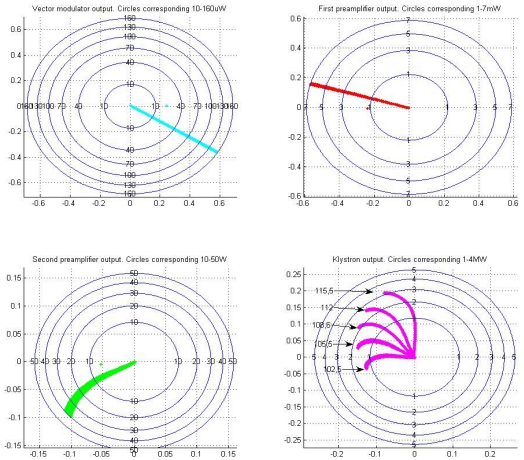


Fig. Complex representation of the HP chain devices
Example for kly. 5 (each axis unit is an ADC voltage)

Results example – klystron 5

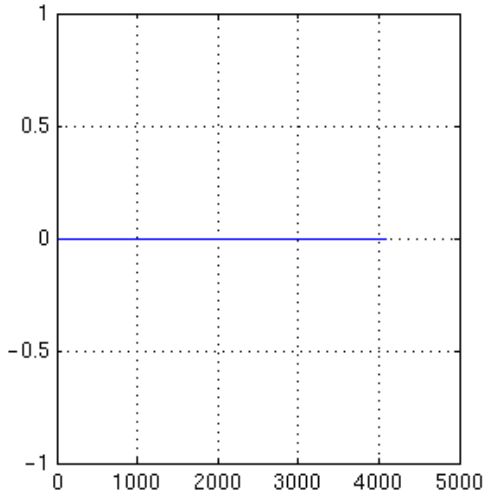


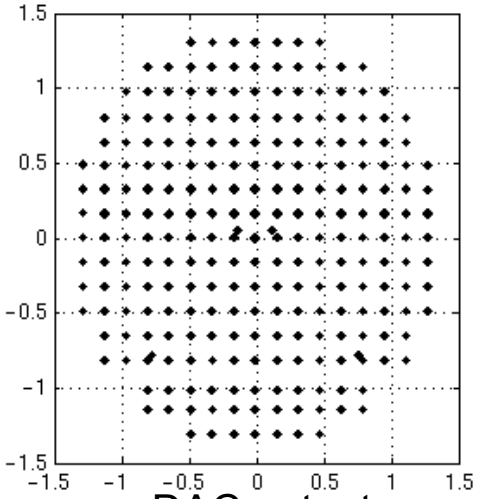
Constellation diagram:
Grid measurement with 20 steps resolution



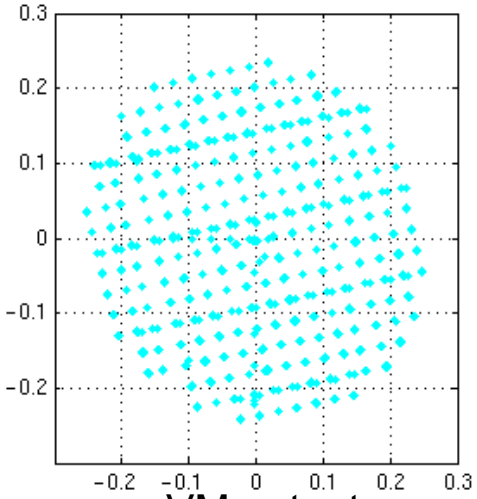
Constellation diagram:
Measurement for one phase - constant Q value (Q=0).
Klystron output characteristics for different HV levels.

KLYSTRON 5

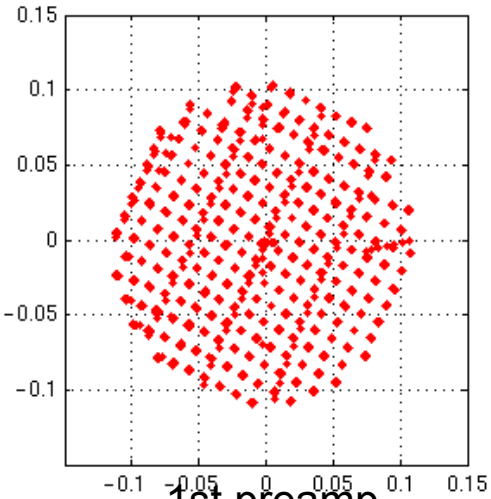




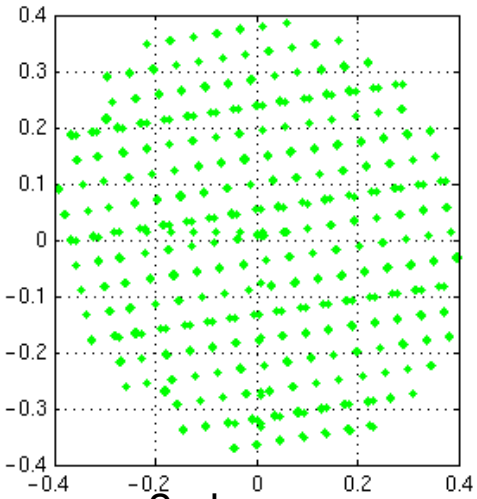
DAC output



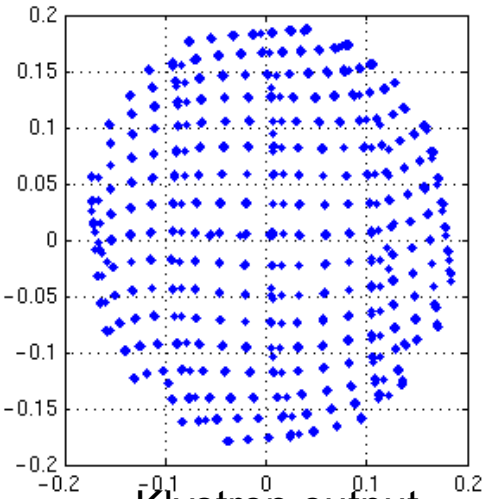
VM output



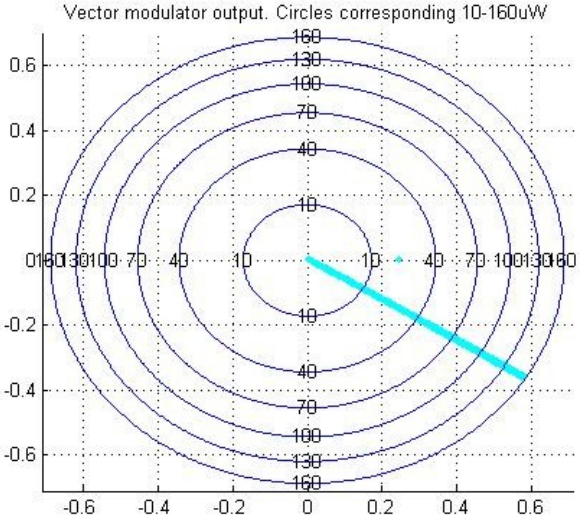
1st preamp

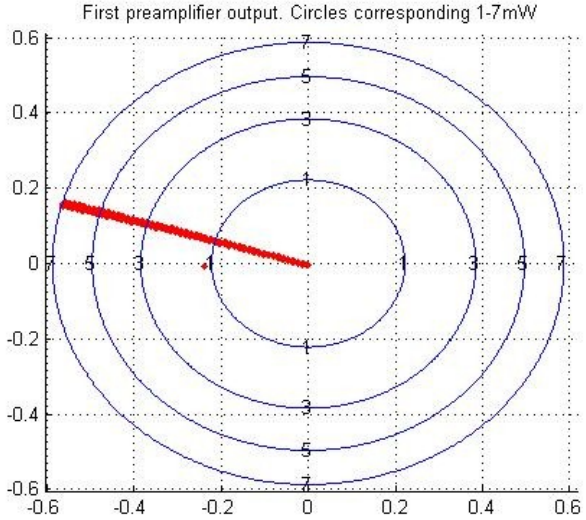


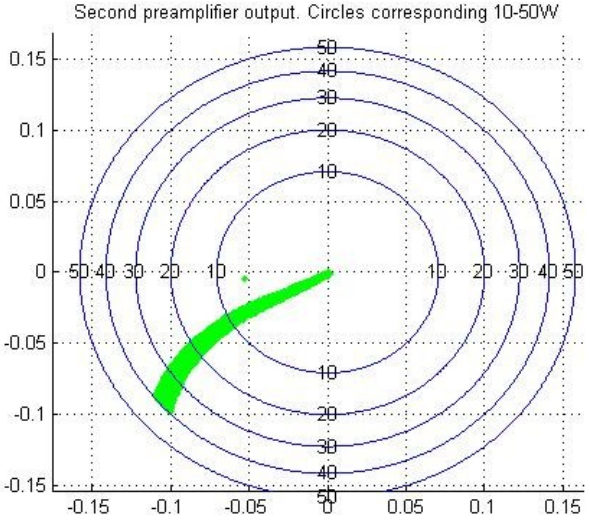
2nd preamp

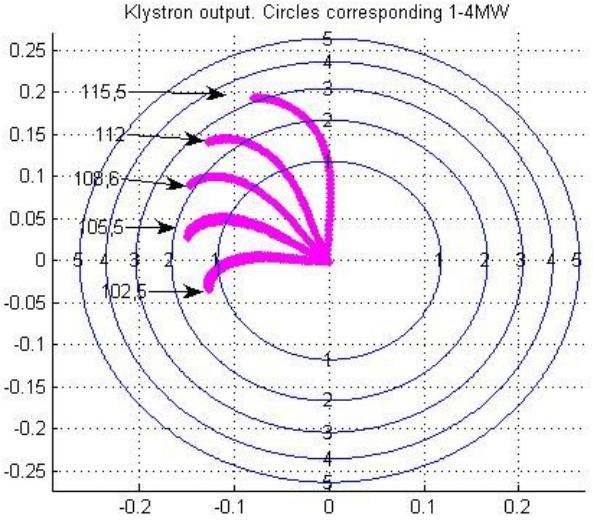


Klystron output

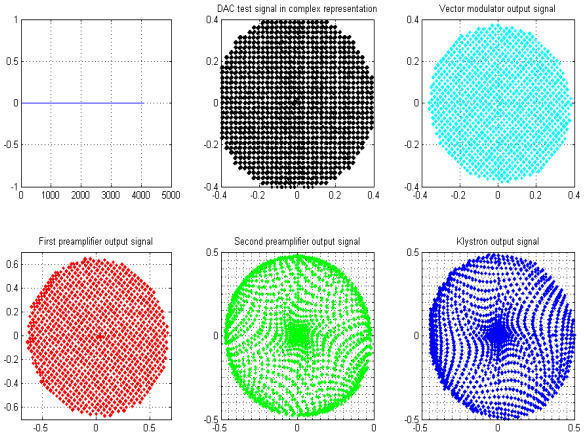

Vector modulator output. Circles corresponding 10-160uW
160
130
100
70
40
10
0.6
0.4
0.2
-0.2
-0.4
-0.6
-0.6 -0.4 -0.2 0 0.2 0.4 0.6


First preamplifier output. Circles corresponding 1-7mW
7
5
3
1
0.6
0.4
0.2
-0.2
-0.4
-0.6
-0.6 -0.4 -0.2 0 0.2 0.4 0.6

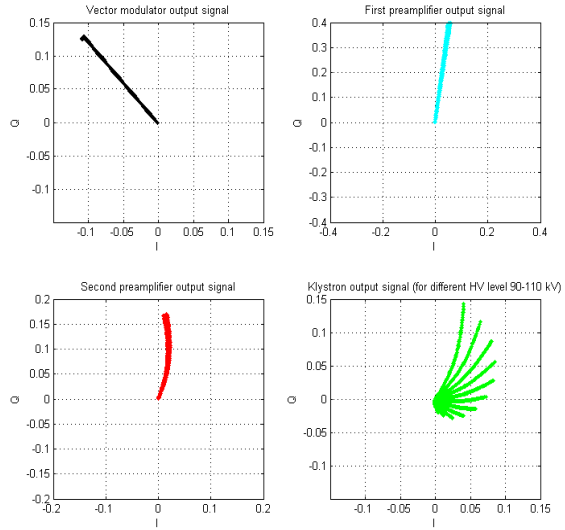

Second preamplifier output. Circles corresponding 10-50W
50
40
30
20
10
0.15
0.1
0.05
-0.05
-0.1
-0.15
-0.15 -0.1 -0.05 0 0.05 0.1 0.15


Klystron output. Circles corresponding 1-4MW
115,5
112
108,6
105,5
102,5
5
4
3
2
1
0.25
0.2
0.15
0.1
0.05
-0.05
-0.1
-0.15
-0.2
-0.25
-0.2 -0.1 0 0.1 0.2

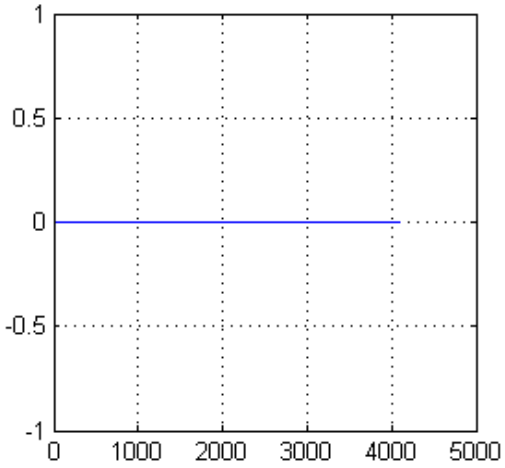
Results example – klystron 2

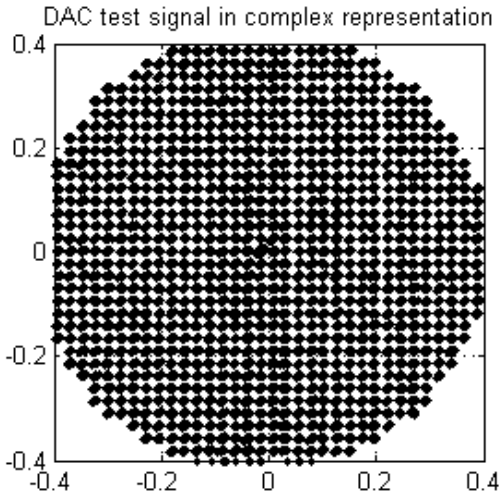


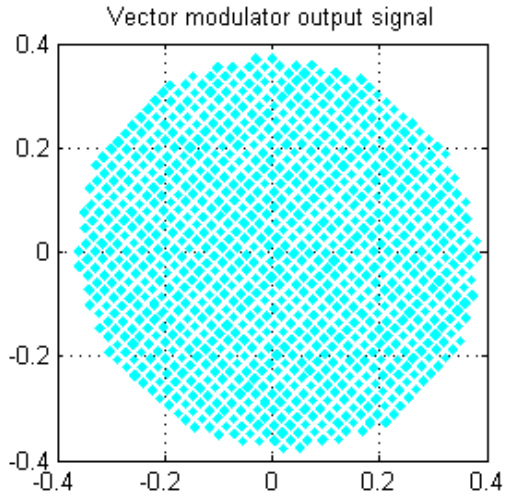
Constellation diagram measurement:
Grid measurement with 50 steps resolution

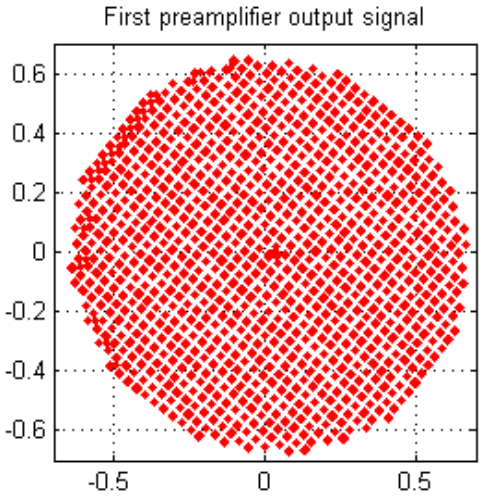


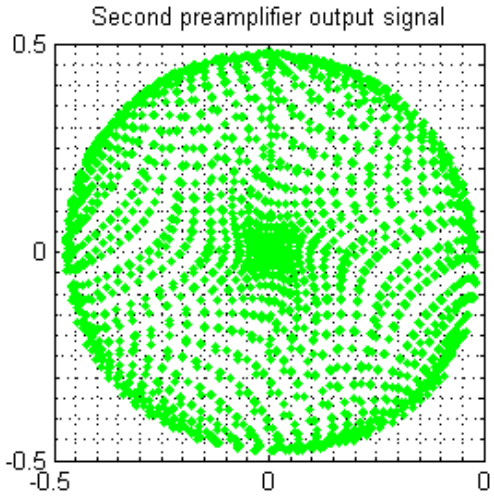
Constellation diagram measurement:
Measurement for one phase - constant Q value (Q=0).
Klystron output characteristics for different HV levels.
Due to FPGA DAC's output level limitation – input signal range is about half of the regular one.

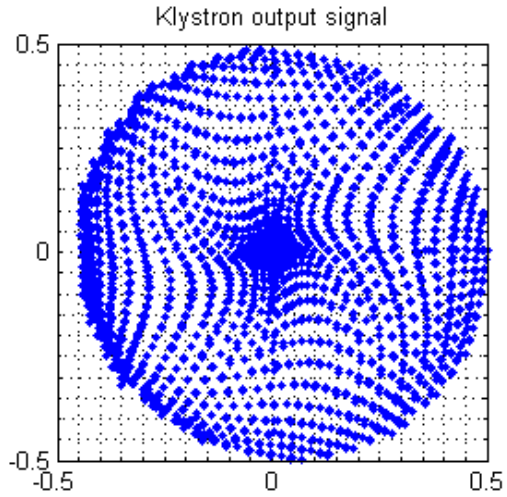

1
0.5
0
-0.5
-1
0
1000
2000
3000
4000
5000

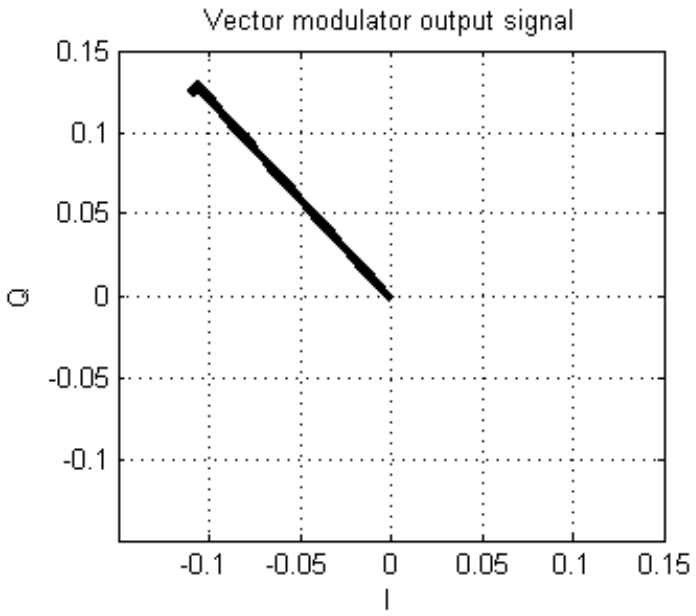

DAC test signal in complex representation
0.4
0.2
0
-0.2
-0.4
-0.4
-0.2
0
0.2
0.4

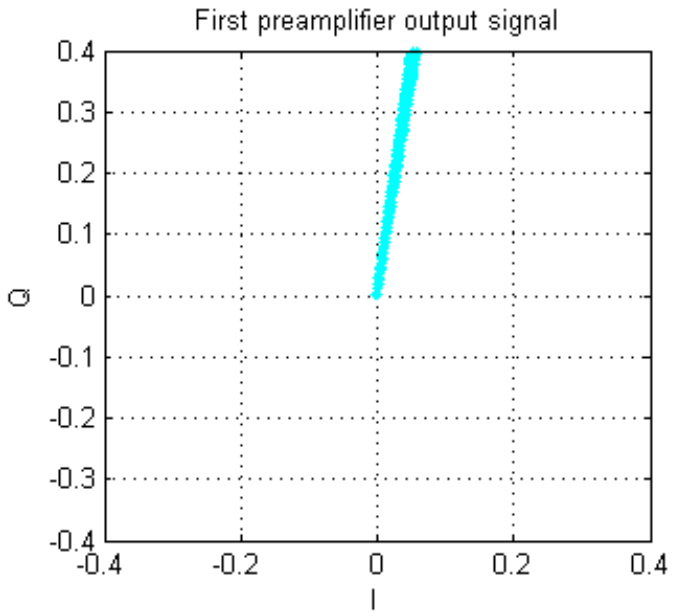

Vector modulator output signal
0.4
0.2
0
-0.2
-0.4
-0.4
-0.2
0
0.2
0.4

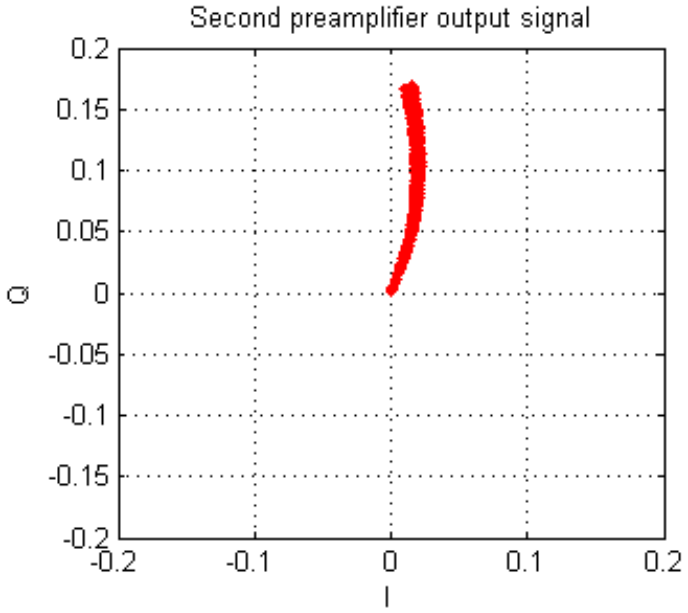

First preamplifier output signal
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.5
0
0.5

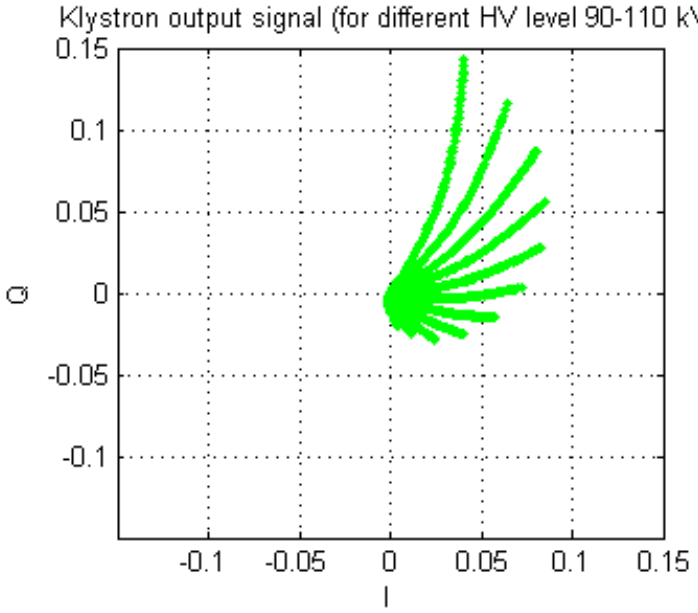

Second preamplifier output signal
0.5
0
-0.5
-0.5
0
0


Klystron output signal
0.5
0
-0.5
-0.5
0
0.5


Vector modulator output signal
0.15
0.1
0.05
0
-0.05
-0.1
Q
-0.1
-0.05
0
0.05
0.1
0.15
I


First preamplifier output signal
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
Q
-0.4
-0.2
0
0.2
0.4
I

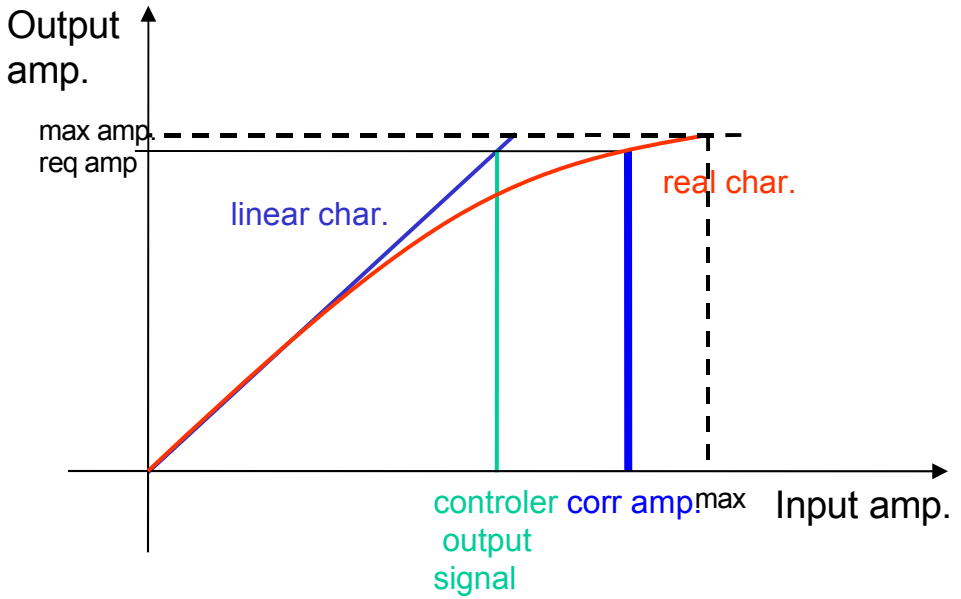

Second preamplifier output signal
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
Q
-0.2
-0.1
0
0.1
0.2
I


Klystron output signal (for different HV level 90-110 kV)
0.15
0.1
0.05
0
-0.05
-0.1
Q
-0.1
-0.05
0
0.05
0.1
0.15
I

Linearisation algorithm

From the non-linearity measurement the AM/AM (amplitude to amplitude) and PM/AM (phase to amplitude) of the high power chain can be achieved.

NOTE!! The nonlinearity is only function of input amplitude.



Driving signal representation:

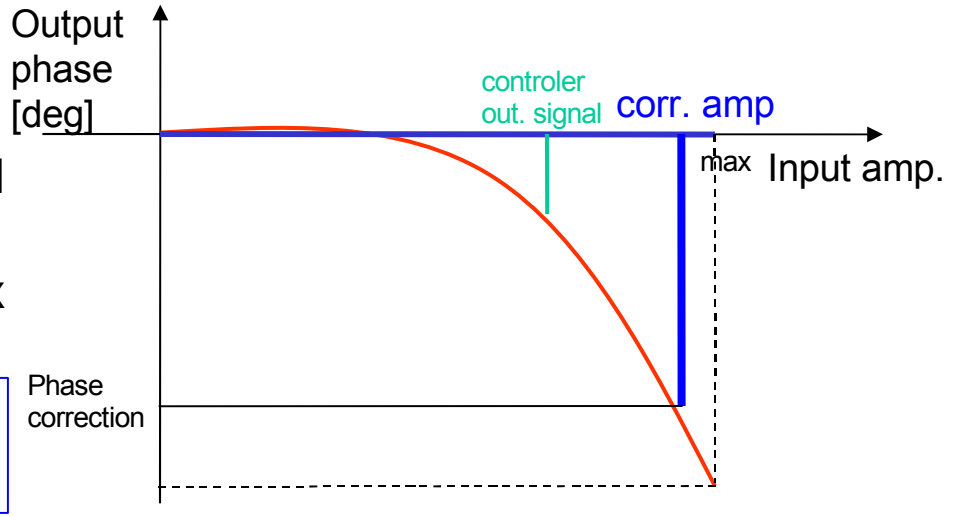
$Z = Id + Qd = |Z| * [\cos(phi) + i * \sin(phi)]$

Correction signal:

$C = Ic + Qc = |C| * [\cos(th) + i * \sin(th)]$

From the linearisation both amplitude and phase correction are achieved.

Can be realised using the complex multiplication.



$C*Z = Idc + i*Qdc$

$C*Z = ||Z|*|C||*[\cos(phi+th)+i*\sin(phi+th)]$

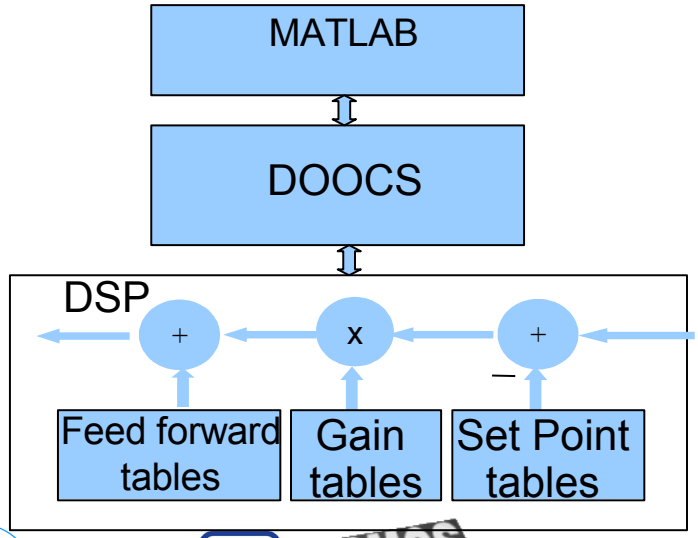
Linearisation algorithm FPGA Simcon and DSP realisation.

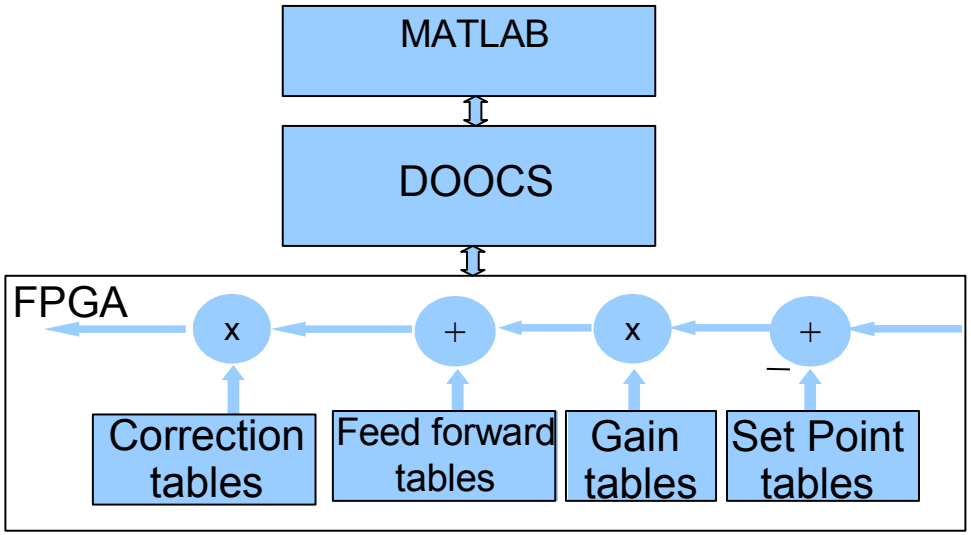
DSP realization:

- correction tables calculated in Matlab,
- controller signal correction performed in Matlab (Feed Forward tables correction),
- correction possible from pulse to pulse (FF tables can be read and write in gap between pulses)
- DOOCS server provided for Feed Forward tables modification and monitoring signals read-out's.

FPGA Simcon realization:

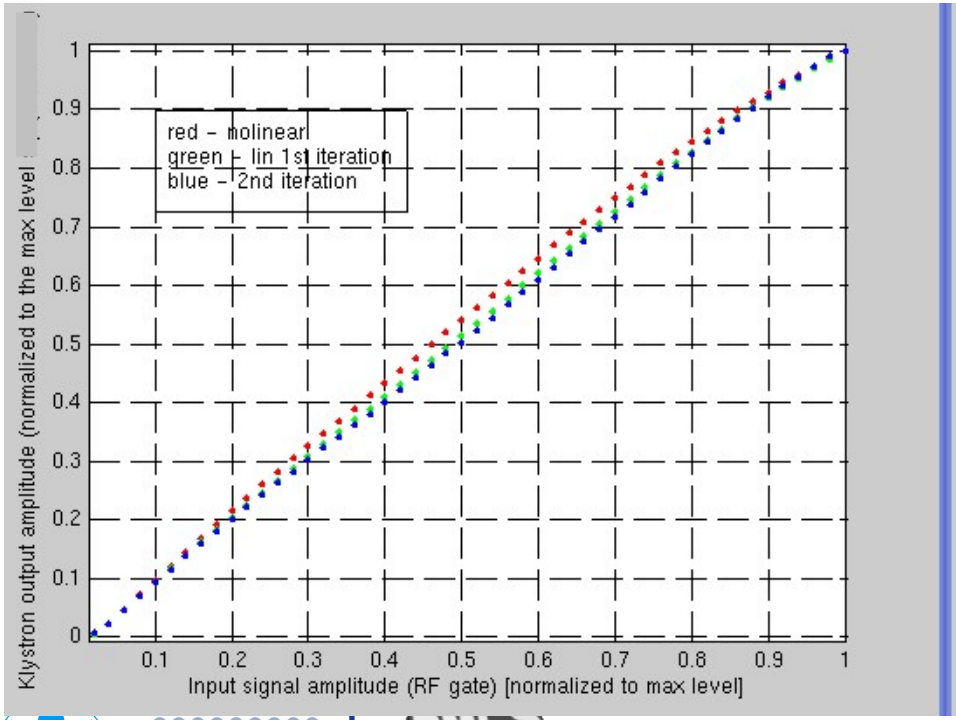
- correction tables calculated in Matlab,
- controller signal correction performed in the FPGA (using: cordic algorithm for amplitude calculation for Ic and Qc tables addressing, and complex multiplication function (WJ)),
- dedicated tables (2048 positions) for I and Q correction vector definition provided (possible slow feedback application)
- correction possible in-pulse to pulse (during the pulse amplitude of each sample generated in open/close loop operation, is corrected)
- DOOCS server provided for tables actualisation (PF)

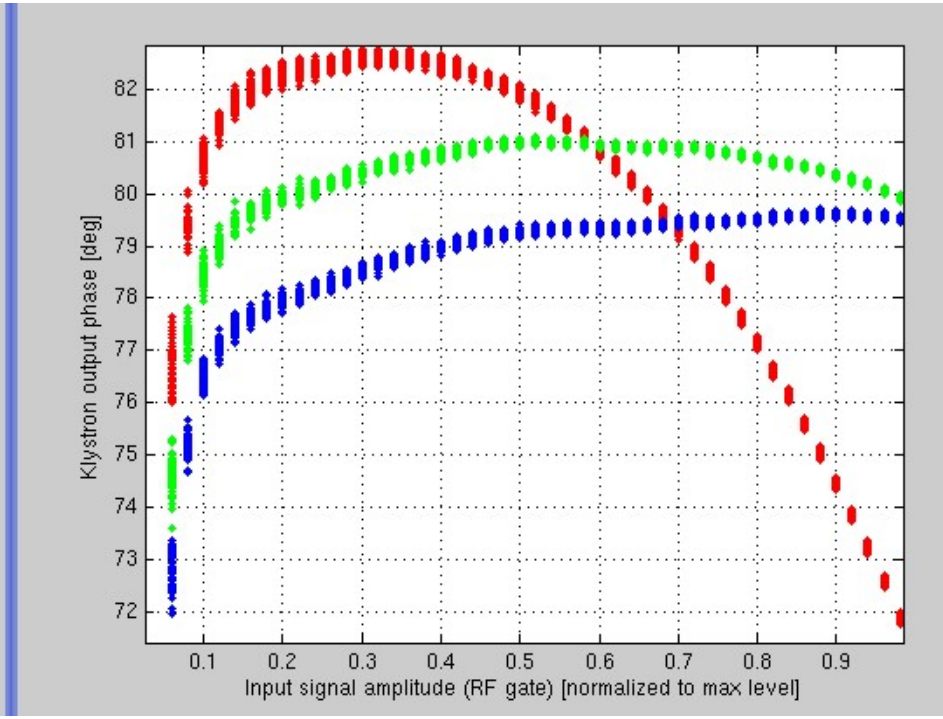




Klystron 5 HPC linearisation results

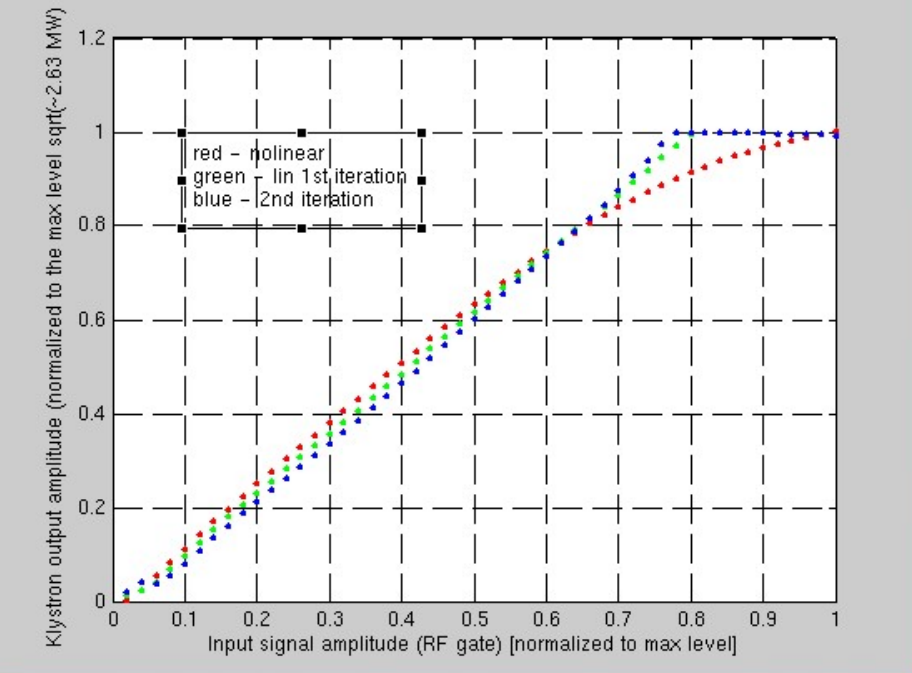
- Linearisation test had been performed using Simcon(FPGA) controler,
- Correction tables were „on”
- HV level – 10800 (value on PLC) about 110kV
- Two iteration of the linearisation were performed.

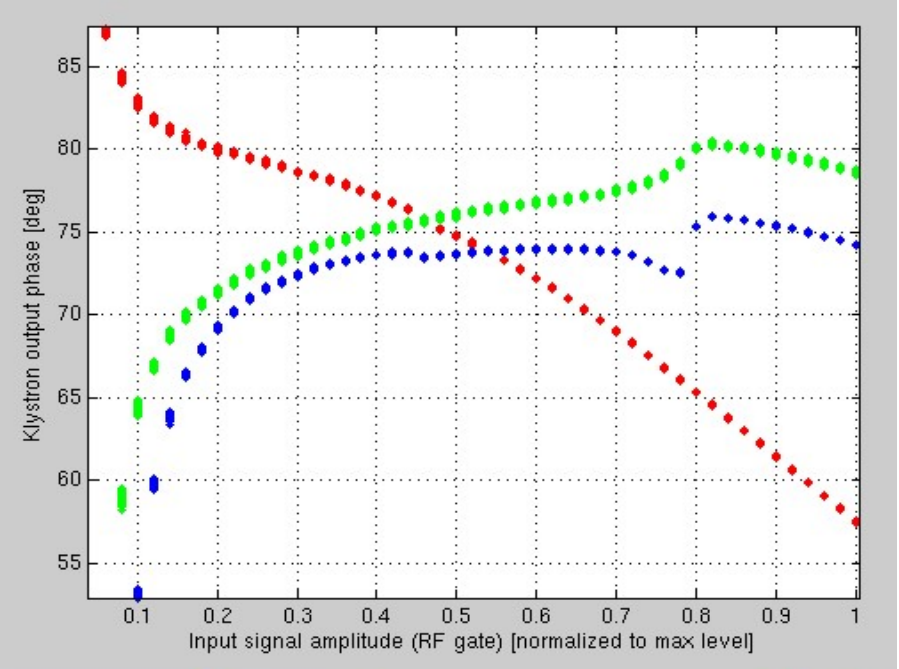




Klystron 5 HPC linearisation results

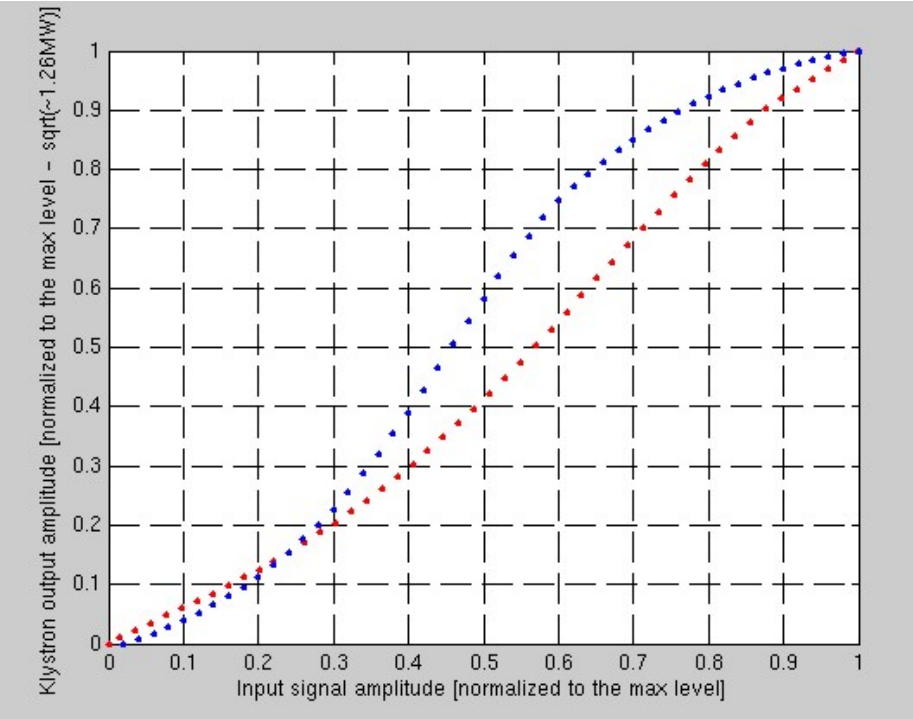
- Linearisation test had been performed using DSP based controler,
- Correction had been applied to the FeedForward Tables
- HV level – 10800 (value on PLC) about 110kV
- Two iteration of the linearisation were performed.

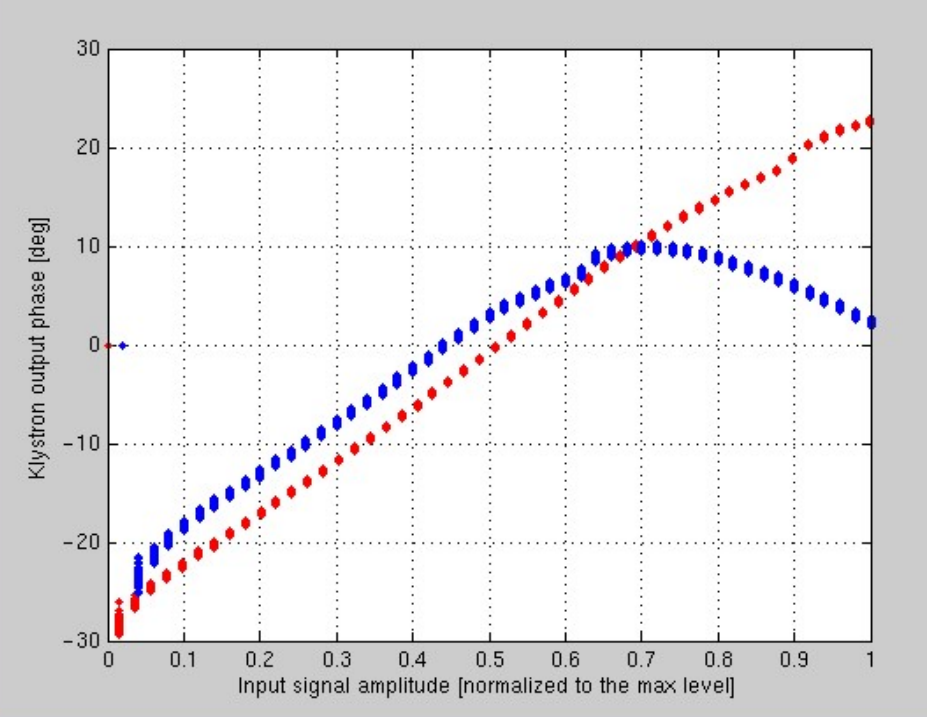




Klystron 2 HPC linearisation results (1/2)

- Linearisation test had been performed using Simcon(FPGA) controler,
- Correction tables were „on”
- HV level – 110 kV
- One iteration of the linearisation were performed.

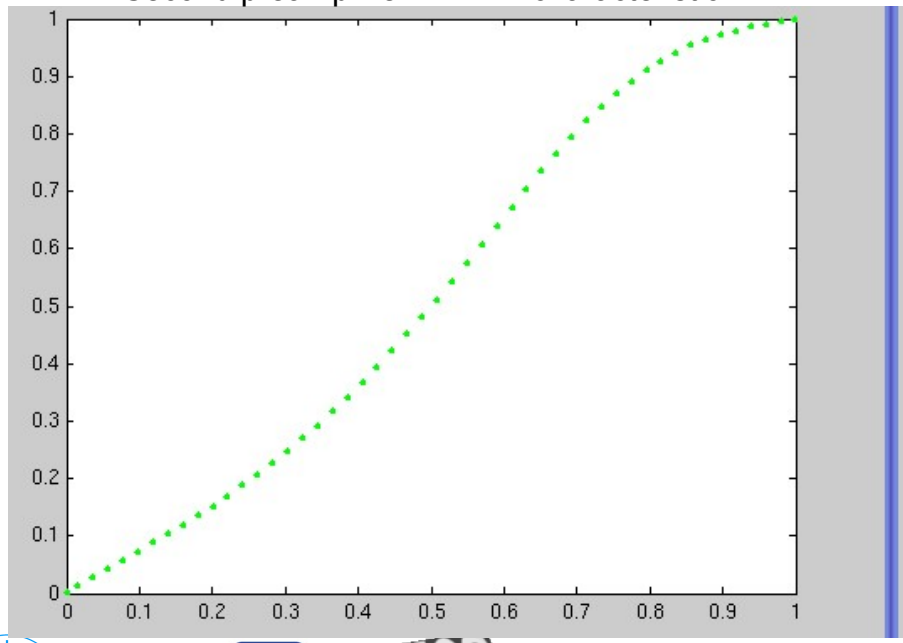




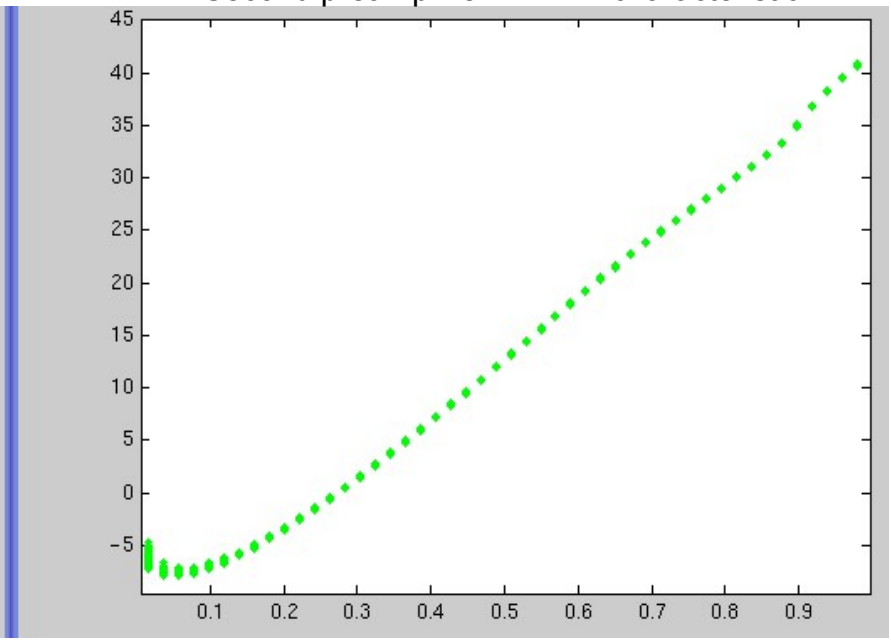
Klystron 2 HPC linearisation results (2/2)

- Strong nonlinearity can be already observed after the second preamplifier.
- Preamplifier exchange from present tube one to this specyfied and ordered by MHF-p should improve situation by factor of 10 or better.

Second preamplifier AM/AM characteristic



Second preamplifier PM/AM characteristic

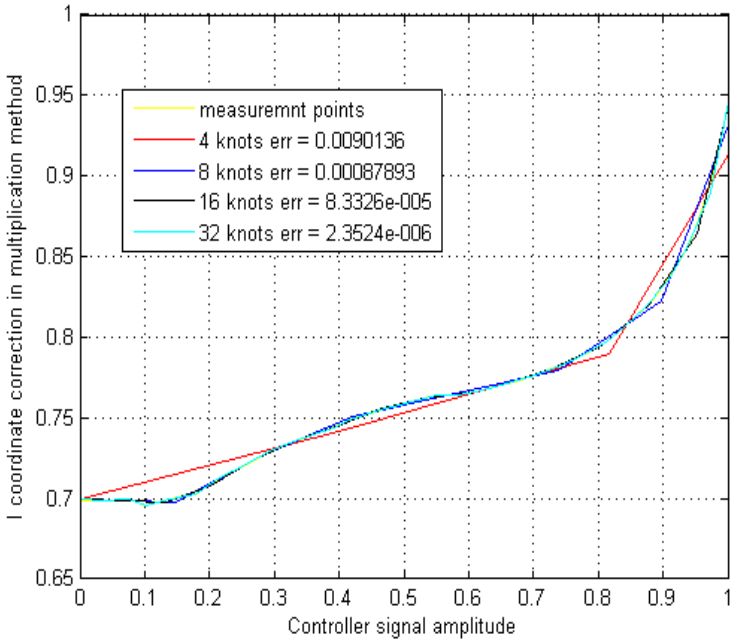


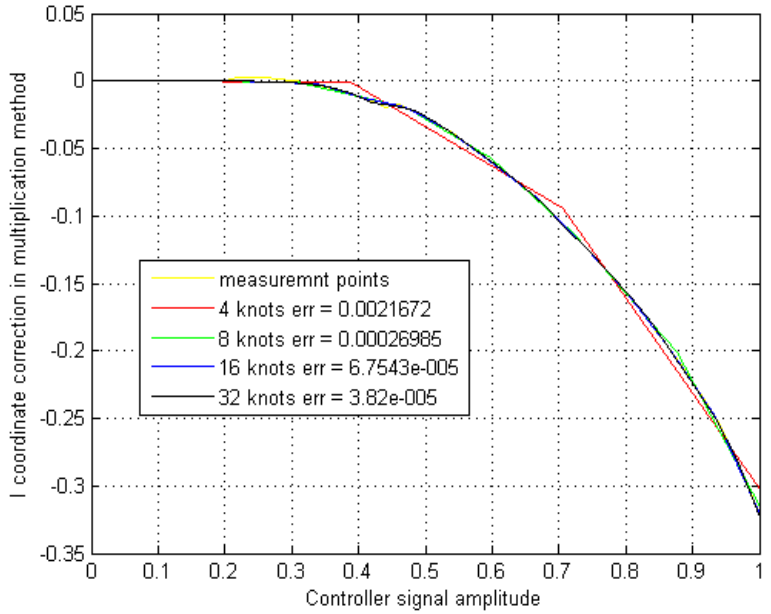
Conclusions

- The linearisation of the klystrons in FLASH can lead to visible amplitude and phase(!) deviation cancellation,
- Using the diagnostics and characterization tool different stages nonlinearities and saturations can be pointed out.
- FLASH does not have (unlikely to the X-FEL probably) problems with klystron saturations for existing high power consumption.
- Linearisation tool have to be improved some of the calculation can be moved from Matlab to the upcoming DSP processor or Power PC (in Virtex II pro), possible slow feedback should be tested – for the tables adaptation.

Next steps – upcoming tests: december.06 (1/2)

- New linearisation method implementation:
  - Signal level calibration after DSP/FPGA change (kly 5 & 2)
  - Performance test of new solution of tables with interpolation (tables size reduction to 32, 16, 8 or 4 words length),





Next steps – upcoming tests: january.07 (2/2)

- New linearisation method implementation:
  - Performance test of new solution of tables with interpolation (tables size reduction to 32, 16, 8 or 4 words length),
- Adaptation algorithm test:
  - MATLAB realisation,
  - Power PC realisation.

Nonlinearity characterization and linearization method tests for klystron 2 and klystron 5

Motivation / Goal:

In order to provide better performance of RF control of klystrons and its preamplifiers the linearisation method for gain compression and phase deviation reduction is needed. In order to check performance of the predistorter linearizer, the test on klystron 2 and 5 are requested.

During the test modules will be operated with Simcon 3.1 based RF controller. The linearizer will be implemented in the Simcon as well.

The goal is to improve high power chain amplitude and phase linearity in the whole input power range (achievable currently by the operators).

Within the December/January studies (ACC1 & ACC2/3):

1. Preliminary characterisation of the klystron nonlinearities (probabely during 12.12.2006 maintenance day).
2. Connection of the Simcon controller to the LLRF loop (acc2&3).
3. Implementing linearizer correction table due to achieved am&ph characteristics.
4. Linearizer work performance test for the different requested input power level.

Remarks:

No 1 The exact time schedule for the individual shifts will be determined from shift to shift, depending on success, unforeseen problems to be solved and boundary conditions set by other studies.

No 2 Tests will be performed for existing HV levels within acceptable input power level range. Due to this restrictions test man not provide the non-linearities characterization and compensation up to the klystron saturation level