TESLA - COLLABORATION

Pulse Generation for TESLA, a Comparison of Various Methods

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Introduction

According to the present planning stage TESLA will be operated by 1200 klystron transmitters which are distributed over the total accelerator length of 30 km. Each of them needs 11 MW input pulse power (nearly 2 % duty cycle, 0.1 s rep rate). To the generation of such pulses with tolerated shape and with adjacent equipment for only small influence on line current variation these methods seem to be suitable:

Voltage sources with pulse transformers

- matched PFN of the delay line type
- mismatched PFN
- "B-Modulator" (Capacitor + Bouncer Circuit)

Voltage source without pulse transformer

- anode modulated klystron and B-Modulator

Current sources with pulse transformer

- SMES (Superconducting magnet energy storage)
- B-SMES (SMES + Bouncer Circuit)

All these systems will be described. A technical design and cost estimation for the referred voltage sources will be given. - All diagrams of electric quantities versus time are SPICE simulations.

1 Specified Quantities

Power Pulse	
Voltage, top	$U_l = 130kV \pm 1$ % during 1.7 ms
Current	$I = 1.835 \times 10^{-6} A/V^{1,5}$
Load resistance, linear	$R_l = 1.51\ k\Omega$
Repetition rate	$T = 0.1\ s \doteq 10\ Hz$
Pulse width*	$T_p = 2\ ms$
Current, average value*	$\overline{I} = 1.72\ A$
Pulse power, peak value*	$\hat{P}_p = 11.18\ MW$
Pulse power, average value*	$\overline{P}_p = 223.6\ kW$
Pulse energy*	$W_p = 22.36\ kWs$

* for rectangular pulse shape and linear load resistance

The pulse generator losses (charging circuits excluded) per pulse should not exceed 2 % W_p. The total line current variation has to be within 2 % compared to the average value.

Lifetime of all components:	$\geq 1.5 \times 10^9$ pulses
Number of klystron arcs during lifetime	3×10^3

The rise and drop times of the pulses are of no importance with respect to the transmitter function but should be kept small — one order of magnitude or less shorter than the pulse duration — to restrict the electric losses. Pulse generation for the methods using pulse transformers is done on such a voltage level that limits the reverse voltage of semiconductor switching to values $\leq$ 11.5 kV. Dissipated energy of shorted klystron: $\leq$ 20 Ws.

2 Delay Line PFN

With regard to the flatness of the pulse top and to the rise and drop time we fix the following parameters:

Pulse transformer		
	leakage inductance 0.5 mH	on 10 kV level
	main inductance $\geq$ 2 H	on 10 kV level
Ladder network		
N = 20 sections	20 capacitors	of equal size
	19 reactors	of equal size
	1 reactor	for adjustment and short circuit damping

Using $\alpha = \dfrac{Z}{R_\ell}$ (R_ℓ: load resistance, Z: characteristic impedance of the PFN) as degree of mismatching we get the following expressions in terms of α (U_0: charged voltage):

capacitors, total stored energy	$\hat{W}_c = \frac{(1+\alpha)^2}{4\alpha} \times W_p$
residual voltage	$U_r = U_0 \frac{1-\alpha}{1+\alpha}$
air core chokes	$\hat{W}_{\ell\ell} = \frac{\alpha}{4} \times W_p$
iron core chokes	$\hat{W}_{\ell fc} = \frac{1+\alpha}{4} \times W_p$

The size of the iron core chokes considers the short circuit current $I_k(\alpha)(I_{k0}$: short circuit current for $\alpha = 1)$

$$I_k(\alpha) = I_{k0} \frac{1+\alpha}{2\alpha}$$

The comparison of 2 values for α: $\alpha = 1$, matched PFN and $\alpha = 0.4$ for $U_0 = 10$ kV shows:

	$\alpha = 1$	$\alpha = 0.4$
Load voltage U_ℓ	5 kV	7.14 kV
Residual voltage U_r	0	4.3 kV
$\hat{W}_c/W_p$	1	1.225
$\hat{W}_{\ell\ell}/W_p$	0.25	0.1
$\hat{W}_{lfe}/W_p$	0.5	0.35

The practical realization makes additional criteria necessary. In order to transform these figures into apparatus sizes, see below.

2.1 PFN–Operation

The matched PFN needs only a closing switch, whereas the output current of the mismatched PFN has to be interrupted. Switching off at the "natural moment" minimizes the transients.

After current interruption at the end of the pulse the energy states of the individual components of the PFN are not equal, also in the case of the matched ladder network where "output current zero" does not involve each reactor current also being zero. According to the weak damping due to the specified low PFN losses, the transient voltage and current components did not die out where the next pulse is fired. Fig. 1 shows the original pulse, generated by a matched ladder network and Fig. 2 the second one which is far from meeting the tolerances. Efficient damping of the transients is done by means of diodes, one pole of which is connected together and to the charging source whereas the others lead to different sections of the delay line. The charging currents open the diodes and allow circulating currents to flow, thus damping the transient oscillations, see Fig. 3. In Fig. 4 the second pulse generated by a mismatched ladder network ($\alpha = 0.5$) without diodes is shown; Fig. 5 and 6 show the same pulse after introduction of 5 diodes and charging by a 5 Hz sine half-wave resp. 11 diodes and 25 Hz sine half-wave charge immediately after the pulse. The capacitor voltages for matched and mismatched PFN ($\alpha = 0.4$) are presented in Fig. 7 and Fig. 8 and demonstrate clearly the unipolar voltage strain in the second case and the low value (10 %) of inverse voltage in the first one. A short circuit, direct or as klystron arc, causes 60 % U_0 as inverse voltage. This is without influence on the design of the capacitors because the number of shorts is only a small fraction of the total quantity of pulses.

2.2 Short circuit handling

Fig. 9 shows the interesting quantities of a matched PFN when the klystron was shorted. The pulse transformer ratio in this case is 26 and assuming 100 V as arc voltage we get, using the quantities of the diagram,

$$\frac{4400}{26} \times 100 \times 2.1 \times 10^{-3}\ Ws = 35.5\ Ws > 20\ Ws$$

as energy dissipated in the arc, which exceeds the tolerated value. Therefore a crowbar is necessary. — The semiconductor switch of the mismatched ladder network is able to interrupt the short circuit current a few microseconds after beginning, if IGBT are used, but, because this switching operation is done at an "unnatural" moment transient oscillations of the whole PFN are following, see Fig. 10, showing the capacitor voltages after current interrruption at half pulse width. These inacceptable capacitor strains are suppressed during a lower time interval if the PFN is recharged soon after switching off. This is demonstrated in Fig. 11; charging was done by a 25 Hz sine half-wave. Because a crowbar system is necessary here as measure of the principle of double safety it seems to be favourable to fire the crowbar of a mismatched PFN at each short circuit occurence. - The thyristor switch of the matched PFN needs reverse voltage after the current extinction. It is available by the inverse voltage of the last PFN capacitor, but reduced by the voltage over the pulse transformer reset circuit. A variation of the Fermilab reset circuit design [1] produces enough reverse voltage as shown in Fig. 12. All elements terminating the delay line PFN are presented in Fig. 13. Its input is closed by a clipper diode series connected by a resistor of the value of the characteristic impedance of the PFN as shown above.

3 B–Modulator

This pulse generator, proposed in [2] consists of a lumped positive charged capacitor banc, charged on the voltage U_{10}, series connected to a parallel resonant circuit which is operated during the 2 ms pulse time between a negative voltage and a positive one in such a manner that voltage versus time is nearly a linear function. In Fig. 14 a simplified circuit diagram is presented. The mode of operation of this network is quickly clear if the circuit is assumed to be free of inductance and the parallel resonant circuit replaced be the voltage source $u_2(t)$ where

$$u_2(t) = A(t - 0.5\ T_p) \qquad 0 \le t \le 2ms = T_p$$

Then the current i_ℓ through the linear load resistance R_ℓ is

$$i_\ell = C_1 \left(A - \frac{U_{10} - A(T_c + 0.5\ T_p)}{T} e^{-\frac{t}{T_c}} \right) \qquad T_c = R_\ell \times C_1$$

If $A = \dfrac{U_{10}}{T_c + 0.5\ T_p}$, i_L = coust. = I_ℓ and has the value

$$I_\ell = \frac{U_{10}}{R_\ell \left(1 + \frac{0.5\ T_p}{T_c}\right)}$$

Practical realization has to take into consideration, of course, the series circuit inductance. It has to be smaller than that in the case of ladder networks; 0.3 mH/10 kV is a suitable value.

For the circuit optimization there are several variable parameters:
voltage ratio $\frac{U_2}{U_{10}}$; resonance frequency and impedance $\sqrt{\frac{L}{C_2}}$ of the parallel resonant circuit. As an optimum we found a network design for 140 Hz resonant frequency and having the total stored energy of the threefold pulse energy of 22.3 kWs:

Main capacitor C_1:	60.1 kWs
Resonant circuit, capacitor:	3.5 kWs
dto., reactor :	4.1 kWs
	67.7 kWs

Fig. 15 shows the output voltage. The ideal, loss-free parallel resonant circuit, operated symmetrically, takes up energy during the first half of the pulse, when its voltage is negative. The same amount of energy is returned to the network when the bouncer voltage is positive. In real case the losses of the resonant circuit have to be supplied, either by an external converter or by the main capacitor C_1. The latter method works by firing the resonant circuit asymmetrically and with negative voltage during longer time as positive one. That is how the TESLA Test Facility is presently operated. The decision about the final equipment, however, should take into consideration that an extra power supply increases the options of influence on the pulse shape. The pulse generator needs a — semiconductor — switch, capable of interrrupting the load current and besides a back to back thyristor-diode layout for the parallel resonant circuit. The shape of the forward off-state voltage of the semiconductor switch after current interrruption and without recharge of the main capacitor is shown in Fig. 16; load voltage $U_\ell = 10\ kV$. The influence of the voltage of the transformer reset circuit is negligible in this case. If it is possible, i.e. by application of the resonance method, recharging should begin not before 2 ms after the end of the pulse to reduce the blocking voltage.

Though the semiconductor switch is able to interrrupt the short circuit current very quickly crowbar systems are necessary as stated above. In order to de-energize both parts of the network 2 crowbars are needed. The main capacitor C_1 produces high discharge currents which have to be damped if the crowbar is fired. That may be achieved by application of the series and parallel damping layout shown in Fig. 17, which is low loss in normal pulse operation.

4 Anode-Modulated Klystron

This design concept eliminates the pulse transformer, pulse production is done on high voltage level 130 kV, at which the anode-modulator replaces the semiconductor switch. In case of a klystron short circuit this modulator is not functionning and a high voltage crowbar has to operate. Energy storage may be done in the B-Modulator mode, because one pole of the klystron is definitely grounded. The application of the optimum found out above to the high voltage level gives a nominal rated voltage of 24 kV peak value for the resonant circuit and with that for the thyristor-diode layout.

5 SMES and B-SMES

The SMES-idea is that of a — superconducting — inductor which is normally short-circuited. Only during the pulse time the short is opened and the current is flowing through the load resistor. So far the SMES-principle represents the inverse network as current source compared

to the capacitor–resistor–network as voltage source. But the real circuitry contains series inductance — mainly the pulse transformer leakage inductance — and parallel inductance in the form of the main inductance of that transformer. Both are influencing the pulse forming in quite another manner as in the case of the voltage source:

Series inductance: The impressed current must be commutated via a parallel connected capacitor, which serves as voltage source. (That is independent of the function of the semiconductor switch.) This process destines the rise of the pulse.

Parallel inductance: The parallel inductance affects the top of the pulse. Instead of the SMES inductance L a parallel connection of that inductance and the transformer main inductance L_h is now effective in this rough estimation.

Assuming the load resistance R_ℓ being linear, the load current i_ℓ in absence of series inductance is:

$$i_\ell = I_0 e^{\frac{t}{T^*}},$$

where $T^* = \frac{n}{n+1}T; \quad T = \frac{L}{R_\ell}; \quad n = \frac{L_h}{L}.$

If the basic time constant T = 0.1 s is to meet the tolerance of the top −2 % after 2 ms pulse width and n = 3 as a value within reach, we get $T^* = 0.75\,T = 0.075$ s and after 2 ms $i_\ell = 97.4\ \%\ I_0$. The conclusion of this is that current sources have to store more energy than voltage sources and the transformer main inductance has to have a minimum value. Another solution is the use of a bouncer–SMES. This is the inverse network as current source compared to the bouncer–capacitor circuit as voltage source. Instead of a parallel resonant circuit the B–SMES has a series resonant circuit, see Fig. 18, the impedance of which $\sqrt{\frac{L_2}{C_2}}$ has to be adapted by an additional pulse transformer in order to avoid excessive voltages. Simulations of such networks demonstrate that it is possible to produce tolerated pulses with only little expanded energy storage compared to the B–pulser.

6 Charging Circuits

Superconducting energy storage and pulse production is only economic if many klystron transmitters are supplied by a sole source. In the case of the above referred voltage sources on the other hand there are hardly advantages by combining many single pulse generators into a large one. The capacitors, mainly in the case of the B–Modulator, are of economic size also for single pulse production and the described air core chokes for ladder networks are only feasible for small dimensions. In addition common pulse sources require pulse cables over longer distances which changes the pulse shape also if matched cabling is used. That is different for the charging equipment for the following reasons:

- Large converters, i.e. for 80 modulators, are distinctly less costly per unit than single supplies.
- Multiplex resonant charging [3] reduces the expense for filter equipment.
- Large converters and filter chokes have lower losses per unit than smaller ones.

A possible configuration of the charging circuitry for 80 modulators is presented in Fig. 19. The converter and its low-pass filter are terminated by a distributing system containing 16 outgoing positions, each with a thyristor-protected inductor and a DC-breaker. The reactor serves not only as a part of the resonance charging system but also limits the current in case of a short circuit of the distributing and the cable system. The fast breaker is a combined facility of a vacuum switch and an electric discharge circuit [4], which enables DC current interruption.

The 16 sub-distributors are equipped with 5 closing thyristors and 5 small make-up power supplies to adapt the charging voltage for each modulator individually. The thyristors are closed successively in intervals of $T/5$. In order to put a modulator after having gone out of operation into the same operating stage as the other four a small and simple starting supply is necessary equipped with a line selector for currentless operation (not necessary for matched ladder networks).

The application of the multiplex charging method implicates waiting periods. In the case of ladder networks the transient oscillations after a current interrruption may continue and cause additional inductor losses which are not negligible for mismatched PFN. Fig. 20 shows the current of the choke of middle position within the PFN, $\alpha = 0.4$, for a 80 ms period. As average for all chokes of a couple of 5 PFN we estimate additional choke losses of 20 ... 30 % of their nominal losses.

6.1 Energy stores of the charging circuits

The multiple charging method for m = 5 parts requires a size of the charging inductor of the ladder network of $\hat{W}_{lr} = \frac{\alpha}{4m} \times W_p$. For the variation of the converter output current the restriction yields, see [3]

$$\hat{i}_{a\sim} = 0.337\overline{I}\left(\frac{\omega_f}{m\omega_0}\right)^2 \leq 0.02\overline{I}$$

(ω_f: resonance frequency of the low pass filter, consisting of L_f and C_f;
$m \times \omega_0 = 5 \times 2\,\pi \times 5$ Hz).

The optimal choice of L_f and C_f has to regard the specific costs per unit of stored energy in both elements. Setting 4 as factor of the costs of stored energy $L_f : C_f$ we get as multiples of the pulse energy W_p

capacitors C_f:	31 % W_p
inductor L_f :	7 % W_p

These figures are independent of the type of the pulse generator; the main capacitor of the B-pulser only requires a smaller size $\hat{W}_{lr}$ of the resonance inductor due to its larger capacitance. This is, however, efficient if it is continuously charged by only an inductor, following the converter. To meet the 2 % requirement for the line- or converter current, this choke has to be designed to store 74 % of the pulse energy.

Continuous Charging may be applied advantageously to single charging of high voltage bouncer networks feeding anode-modulated klystrons. To avoid expensive high voltage insulated inductors these are arranged on the primary side of the rectifier transformer, see Fig. 21. Such a system ensures complete separation in case of failure of one modulator or klystron as it is similarly done in all circuits with resonant charging using closing thyristors. The position of the chokes makes it possible to de-energize them by inverter operation of the thyristor converter.

Continous charging with a common converter for many modulators requires additional switches to interrupt each modulator path in failure case. The inductance of the charging reactor limits the rise of the short circuit current.

7 Technical Aspects

The individual components should be designed under the following perspectives:

Semiconductor pulse switches: Only the matched PFN allows application of the well known and cheap thyristor. The other types of pulse generators need a new type of switch, capable of interrupting current on a 10 kV voltage level. IGBT are said to be the future elements. They interrrupt the short circuit soon after its beginning and without any restriction in time after switching on as in the case of GTO. In contrast to these they are short-circuit proof. Conditioned on its structure they are sensitive to thermal swings as they occur in pulse operations. Their amplitude determines the life time of the elements and the allowed temperature gradient which ensures a lifetime of 1.5×10^9 pulses is uncertain until now. It seems that this value has to be below 10 K.

IGBT and their control circuits are of smaller size, they are less costly and need not to be pressed – compared to GTO.

Pulse transformers: The construction of European low frequency power transformers with stacked iron sheets and circular cylindric coils is less expensive and more reliable in operation than usual pulse transformers used for short time (< 0.5 ms) pulse application.

Chokes for delay line type PFN Air core chokes are light-weight and designed independent of any short circuit current. This advantage compared with iron core chokes is prevailing dealing with small sized units, therefore for mismatched ladder networks.

The magnetic stray field has to be considered and an arrangement with parallel coil axes and inverse flux direction is advantageous. Few percent positive coupling between adjacent inductors is of favourable influence on the pulse shape.

Single charging systems: Single charging systems cause more electrical losses, mainly the transformers and inductors of them. Compared to a common converter system feeding 80 modulators we estimate 4 kW as surplus losses for one modulator. Within 40000 operational hours the cost is 24 TDM. Low loss design of the single converters increases the investment costs.

8 Cost Estimation

We found out the costs for one of 1200 modulators, containing the modulator itself, the charging circuit and the primary 50 Hz-3-phase circuit until the next of 16 supply points or shares of them. Thus the delay line type PFN; mismatched, $\alpha = 0, 4$, equipped with air core chokes and with common, multipole charging circuit for 80 modulators is the least expensive system; estimated price: 280 TDM. On this basis the percentage of the surplus costs of the other modulators are estimated to be

a) common b) single charging	a	b
mismatched ladder network, α = 0, 4, air core chokes	0	+28 %
mismatched ladder network, α = 0, 4, iron core chokes	+16 %	+44 %
matched ladder network, air core chokes	+6.5 %	+35 %
matched ladder network, iron core chokes	+23 %	+51 %
B pulser with bouncer power supply	+5.5 %	+31 %
anode modulated system without klystron surplus costs	+79 %	+105 %

9 Conclusion

The cost estimation shows that the costs for 3 modulator types are close together. Two of them are dependent on the behaviour of semi-conductor, current interrupting switches which are not entirely known in the present. Therefore the matched ladder network equipped with air core chokes and a closing thyristor is a welcome reserve.

The operational handling of systems using single charging is simpler than those of common charging but distinctly more expensive.

Experience should be made with prototypes of a

- IGBT semiconductor switch,
- pulse transformer in power transformer construction,
- ladder network with air core chokes.

References

[1] C. Jensen: "TESLA Klystron Protection Circuit", Tech. Note 29.03.93, Fermilab

[2] H. Pfeffer, C. Jensen, S. Hays, L. Bartelson: "The TESLA Modulator", TESLA 93 30. July 1993

[3] W. Bothe: "Optimization of Circuits with Pulse Forming Networks", XVth Int. Conf. on High En. Acc. – HEAC 1992

[4] H. Bonhomme, G. Defosse, B. Kaczmarek: "Der hyperschnelle Schutzschalter", ACEC Zeitschrift Nr. 4, 1987, p.10 – 13

– 21 Figures following —

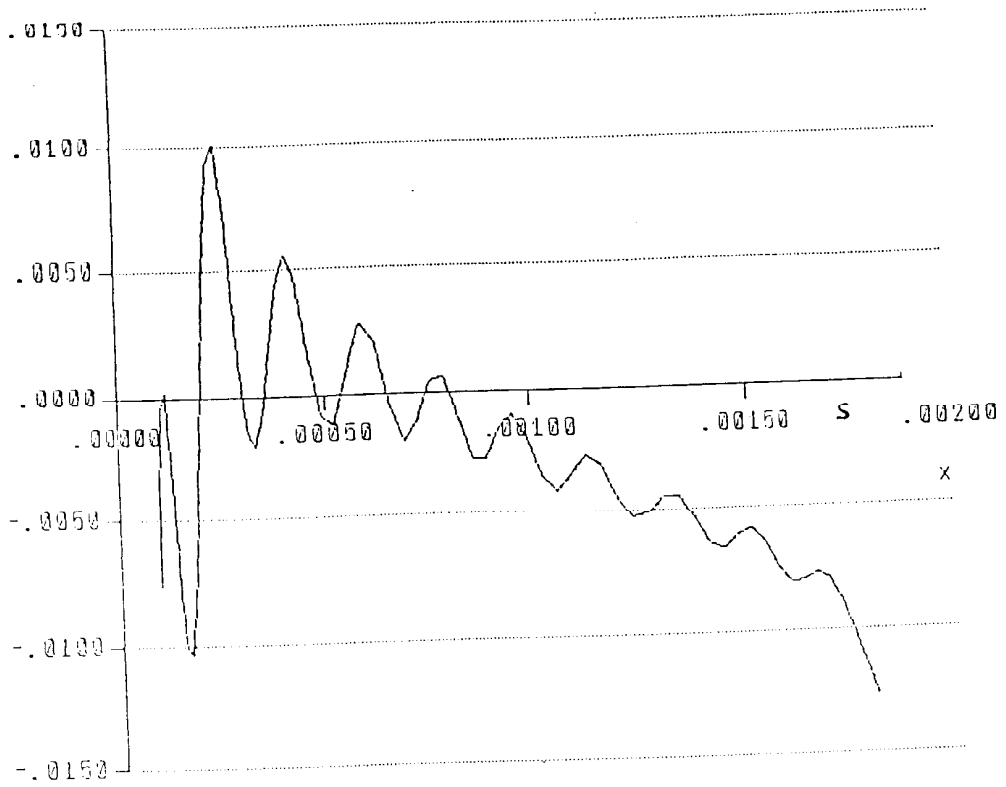

Figure 1. Matched Ladder Network. Original Pulse, Output Voltage U_ℓ. Figured: $\left(\frac{U_\ell}{4903\ V} - 1\right)$ vs. Time

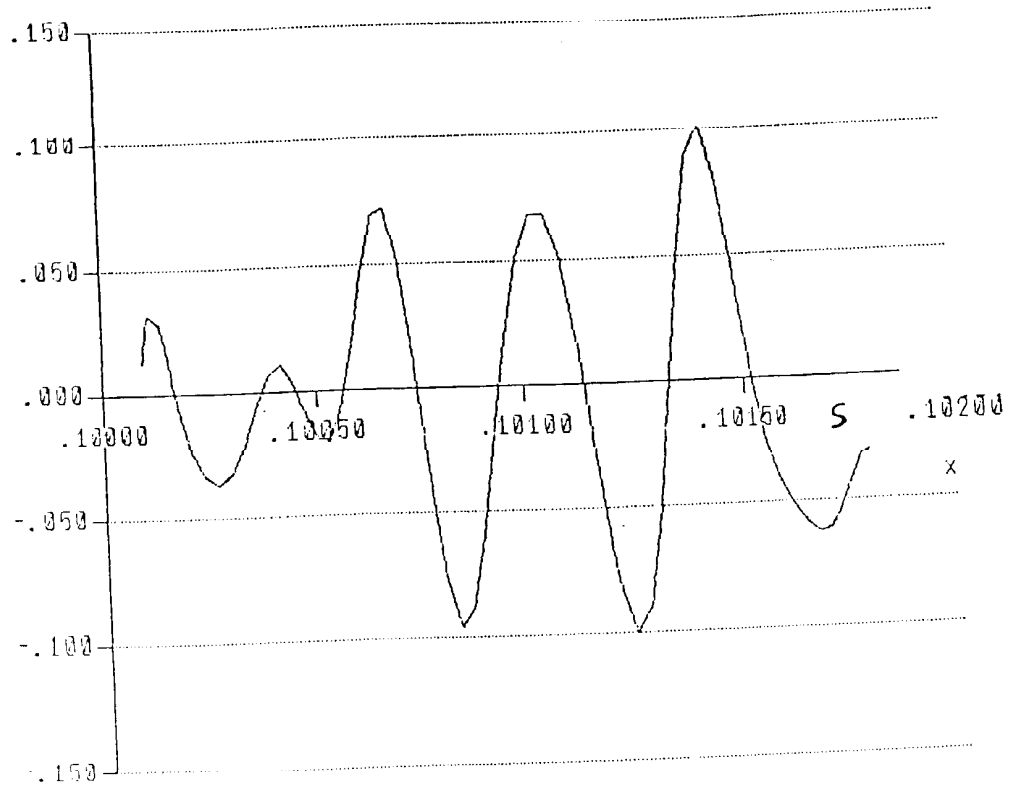

Figure 2. Matched Ladder Network. 2nd Pulse after Recharge, Charge Circuit without Diodes, Output Voltage U_ℓ. Figured: $\left(\frac{U_\ell}{4900\ V} - 1\right)$ vs. Time

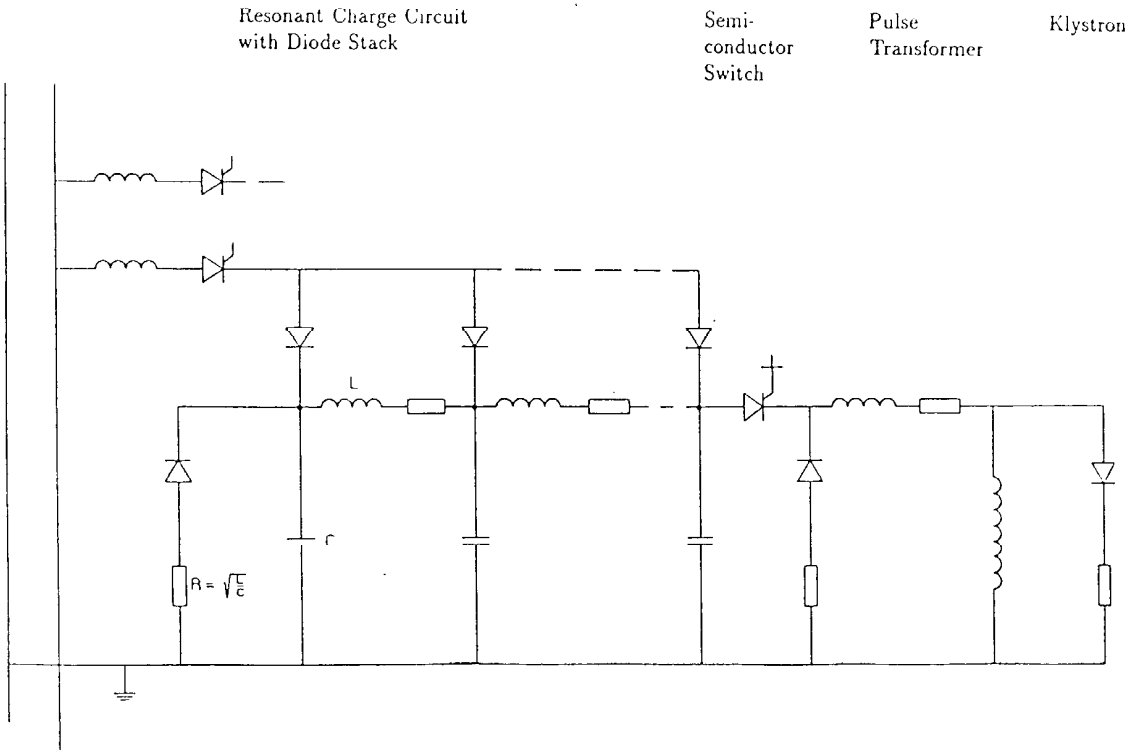

Figure 3. Delay Line PFN — Equivalent Circuit Diagram

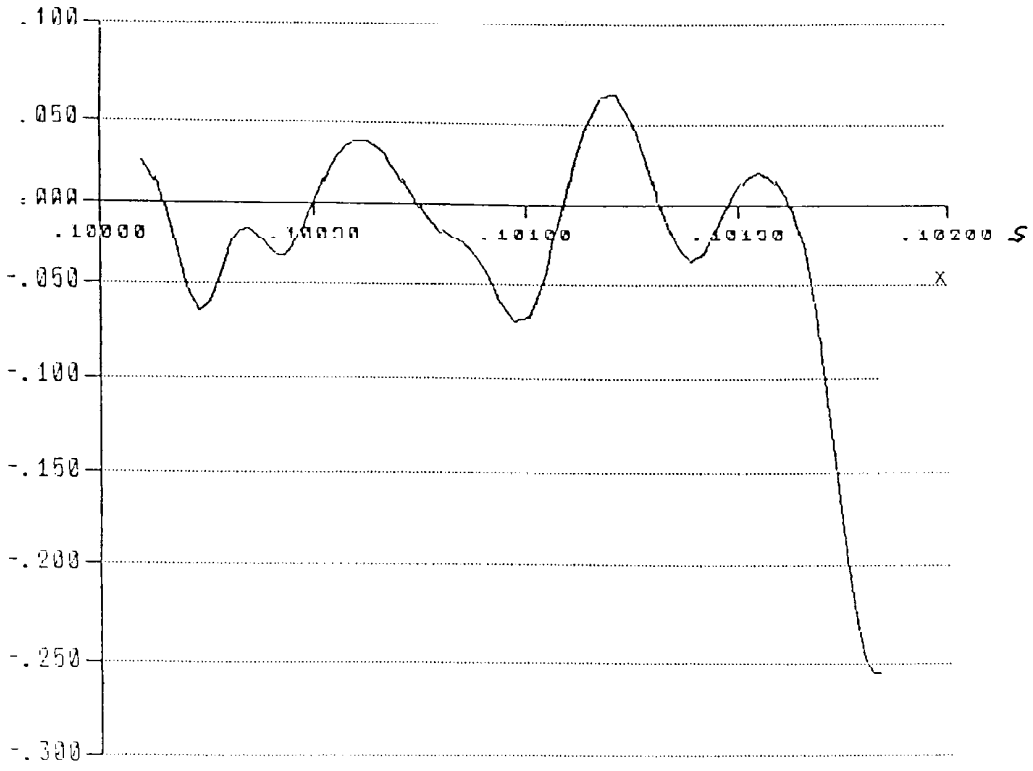

Figure 4. Mismatched Ladder Network, $\alpha = 0.5$. 2nd Pulse after Recharge, Charge Circuit without Diodes, Output Voltage U_t. Figured: $\left(\frac{U_t}{6500\ V} - 1\right)$ vs. Time

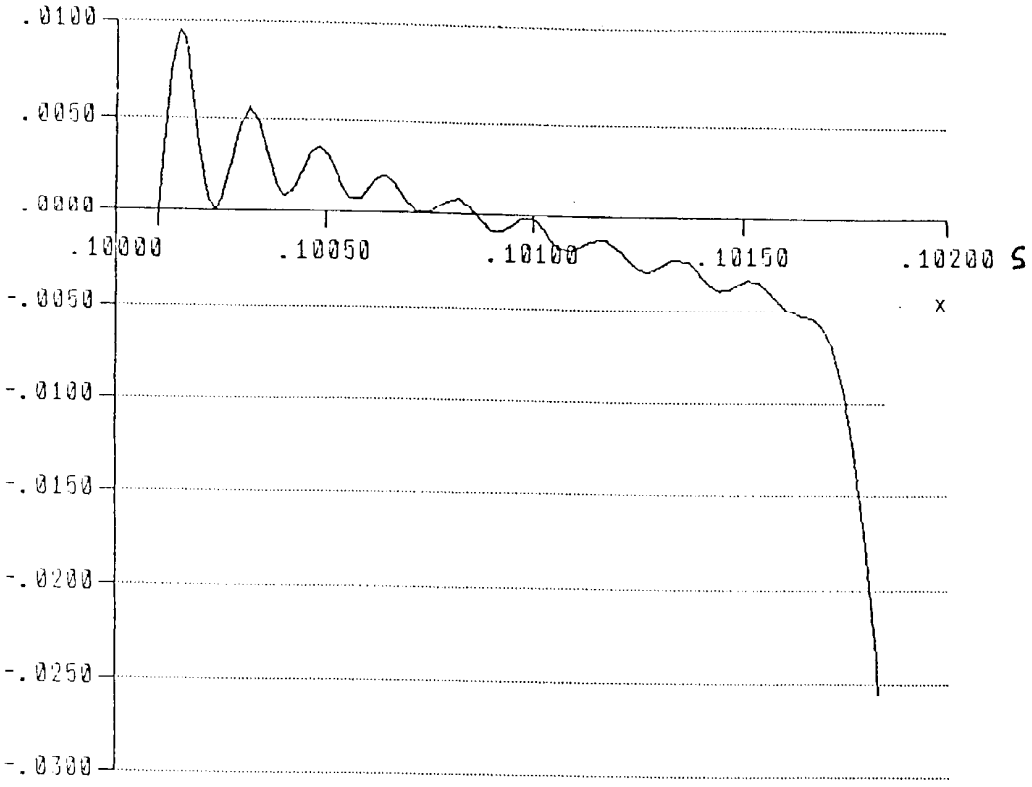

Figure 5. Mismatched Ladder Network, $\alpha = 0.5$. 2nd Pulse after 5 Hz-Recharge with 5 Diodes, Output Voltage U_ℓ. Figured: $\left(\frac{U_\ell}{6570\ V} - 1\right)$ vs. Time

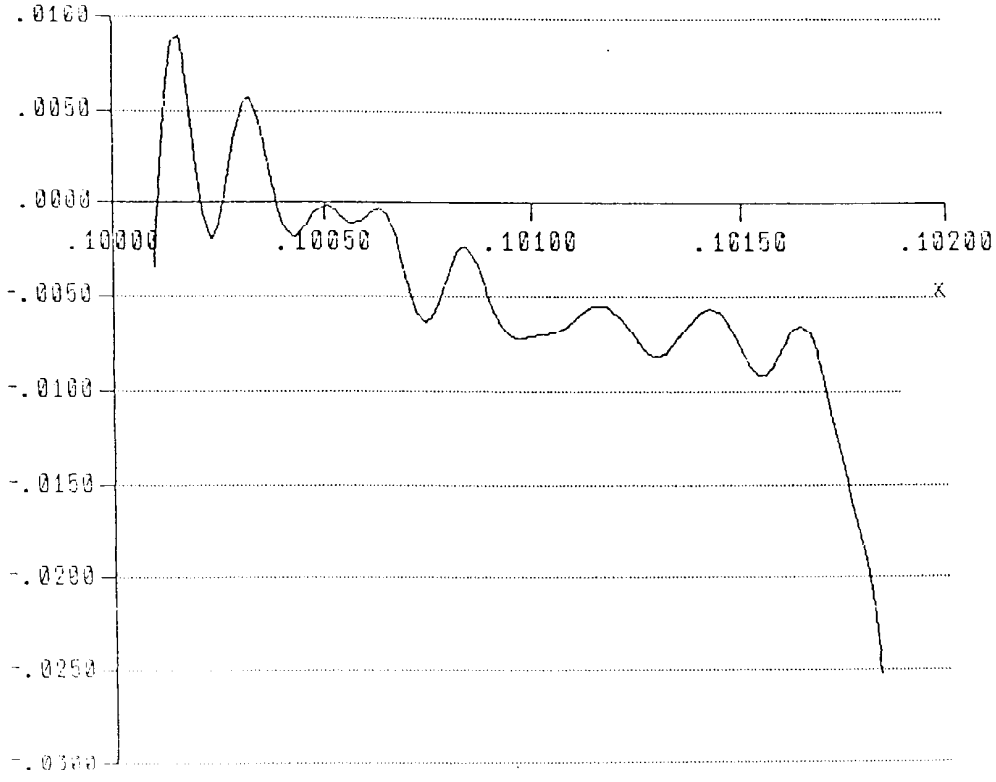

Figure 6. Same Graph as in Fig. 5, but Recharge Frequency 25 Hz; 11 Diodes

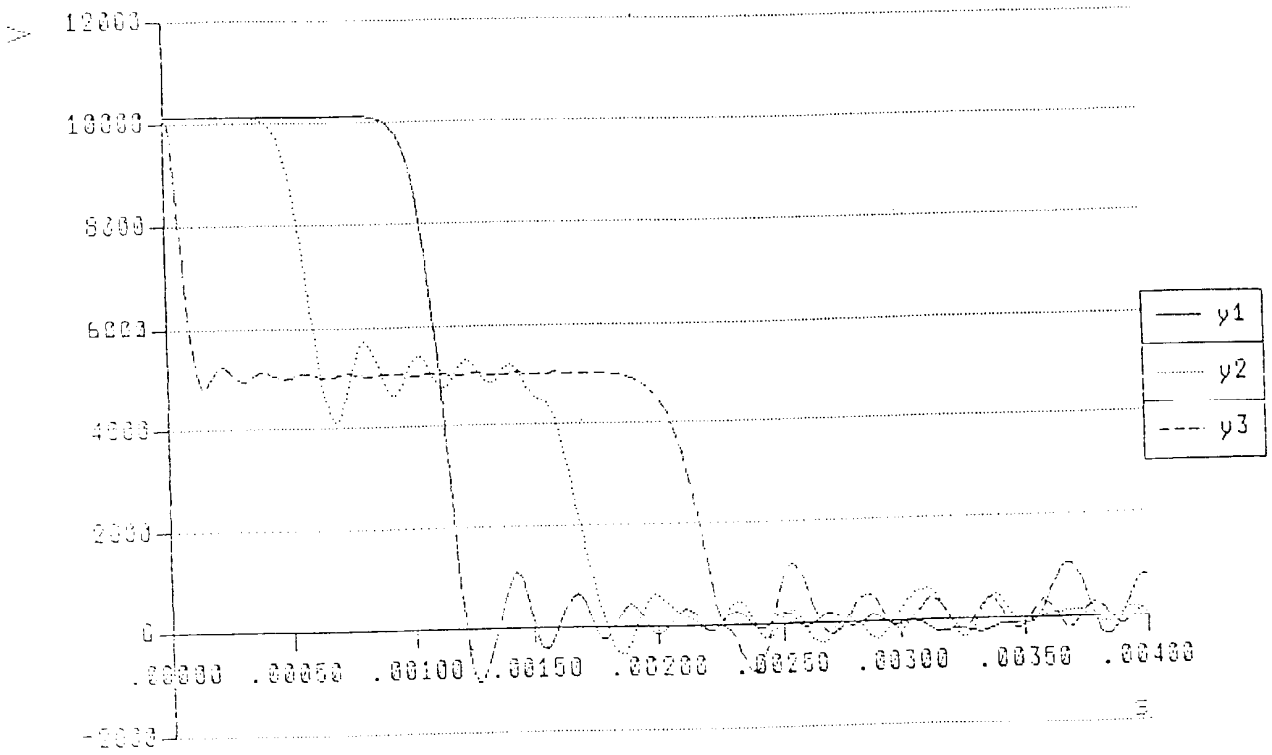

Figure 7. Matched Ladder Network – Capacitor Voltages vs. Time. y1: Initial–, y2: Middle–, y3: End–Position

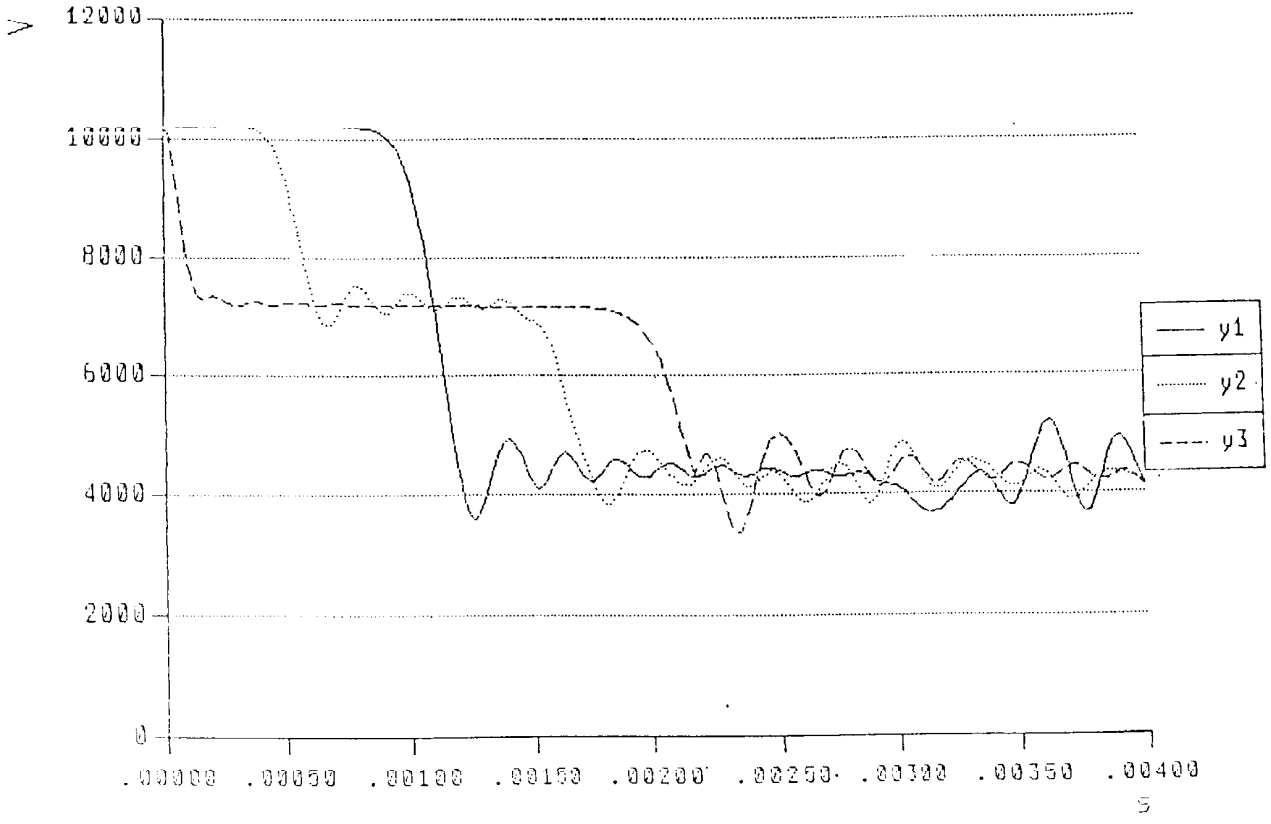

Figure 8. Mismatched Ladder Network, $\alpha = 0.4$. Capacitor Voltages vs. Time. y1: Initial–, y2: Middle–, y3: End–Position

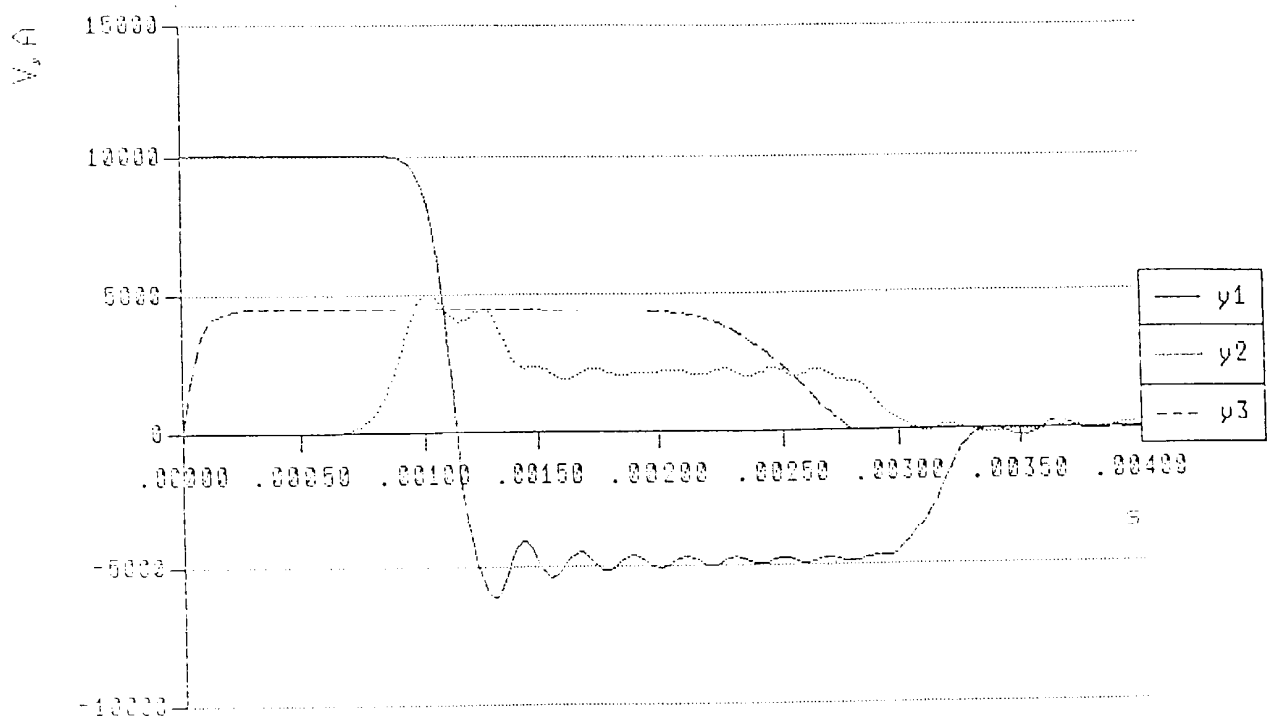

Figure 9. Matched Ladder Network. Load shorted after 1 ms. Output Quantities vs. Time. y1: Capacitor Voltage, Middle Position y2: Choke Current, Position 1/4 y3: Load Current

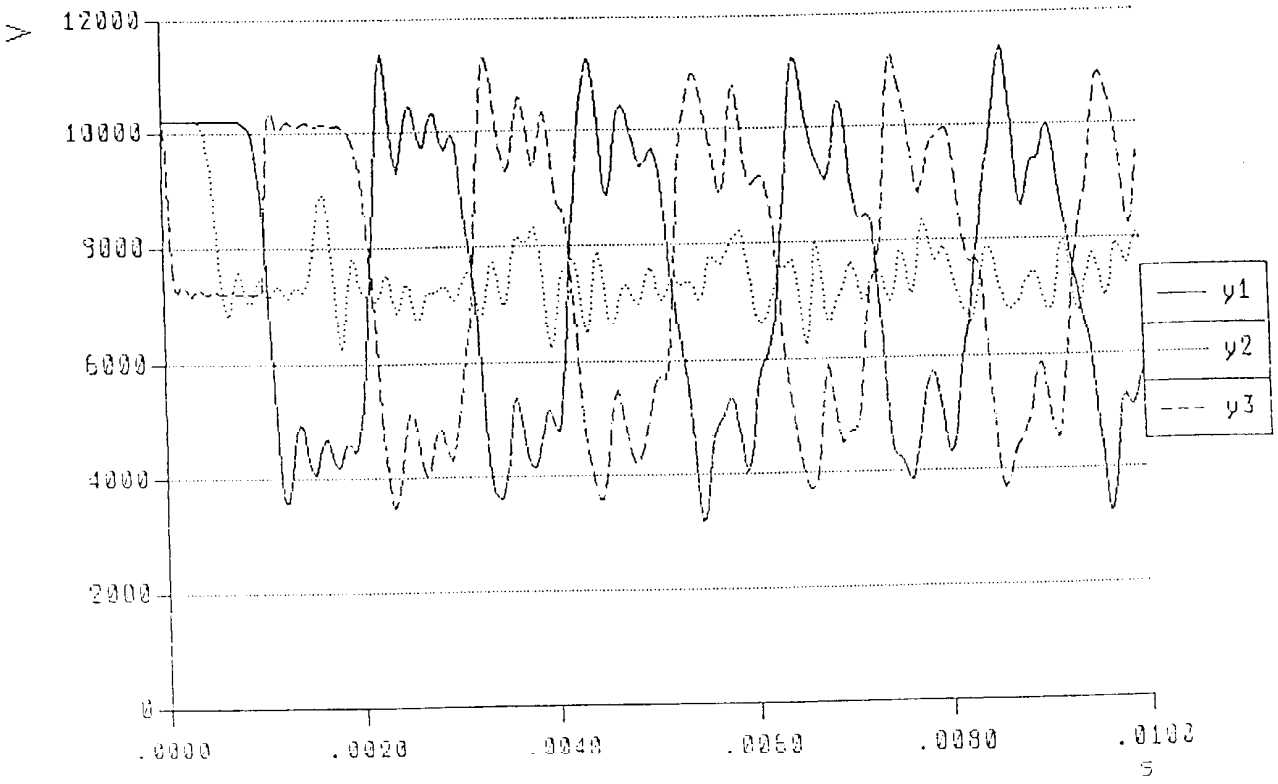

Figure 10. Mismatched Ladder Network, $\alpha = 0.4$. Capacitor Voltages vs. Time after interrrupted Load Short without Recharge. Capacitor Locations: y1: Initial-, y2: Middle-, y3: End-Position

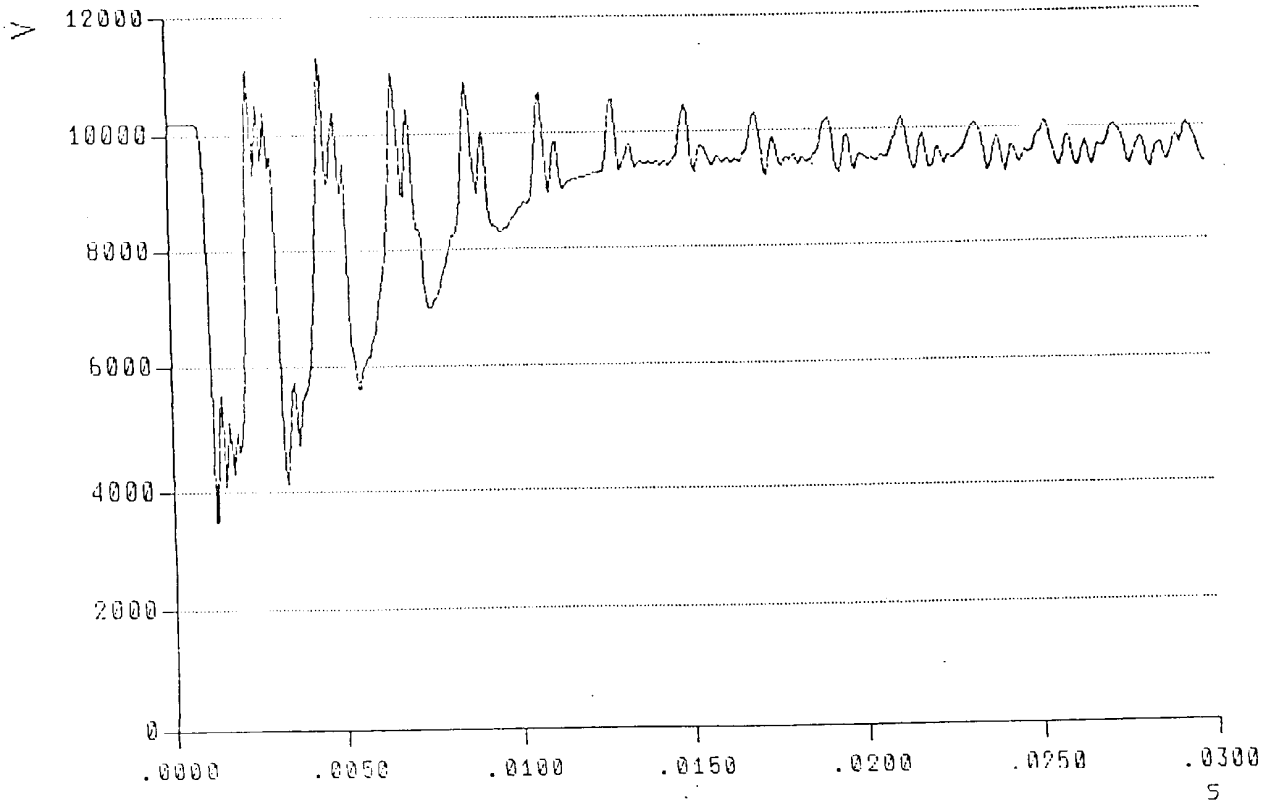

Figure 11. Mismatched Ladder Network, $\alpha = 0.4$. Capacitor Voltage vs. Time after interrrupted Load Short and Recharge. Initial Position.

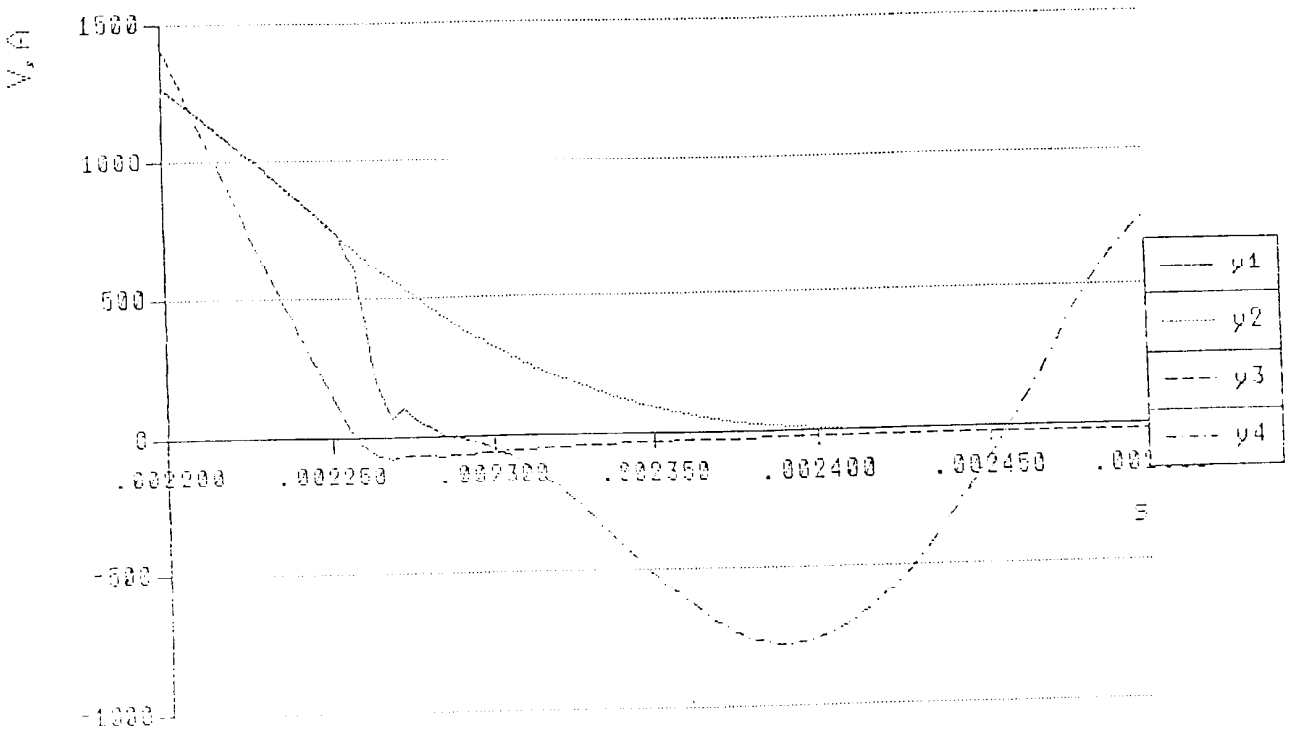

Figure 12. Matched Ladder Network, Output Quantities vs. Time after Pulse. y1: Output Current, y2: Load Current, y3: Pulse Transformer Reset Circuit-Voltage, y4: Thyristor-Blocking Voltage.

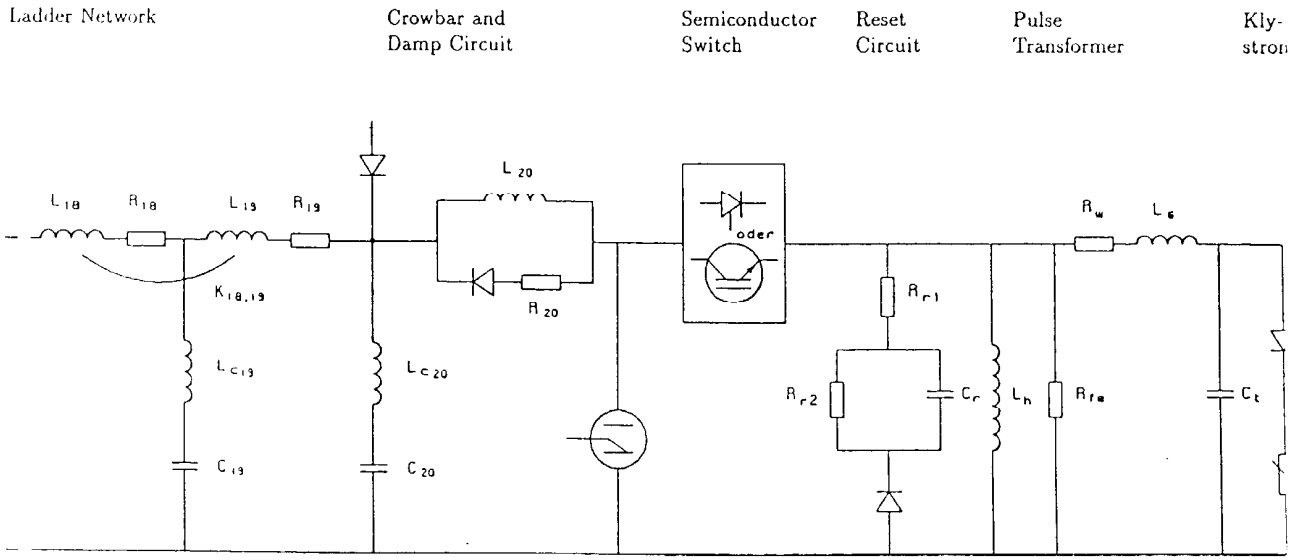

Figure 13. Ladder Network. Last Sections and Termination

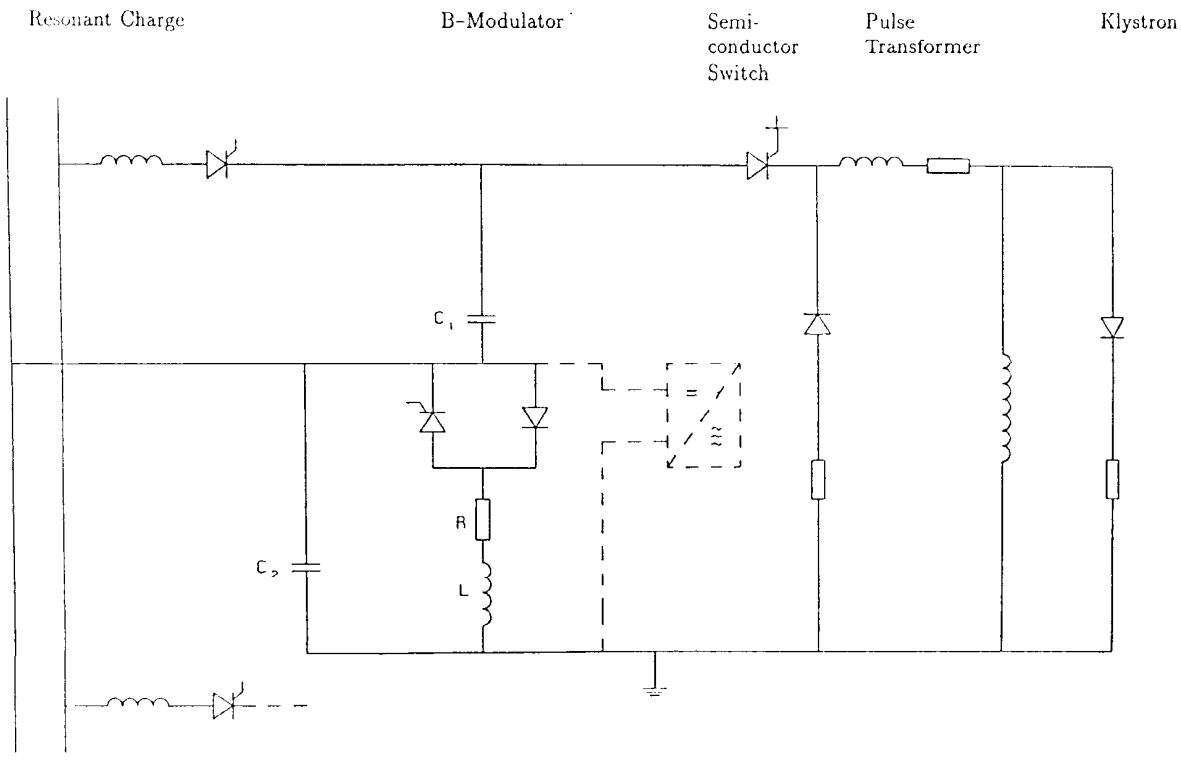

Figure 14. B-Modulator. Equivalent Circuit Diagram.

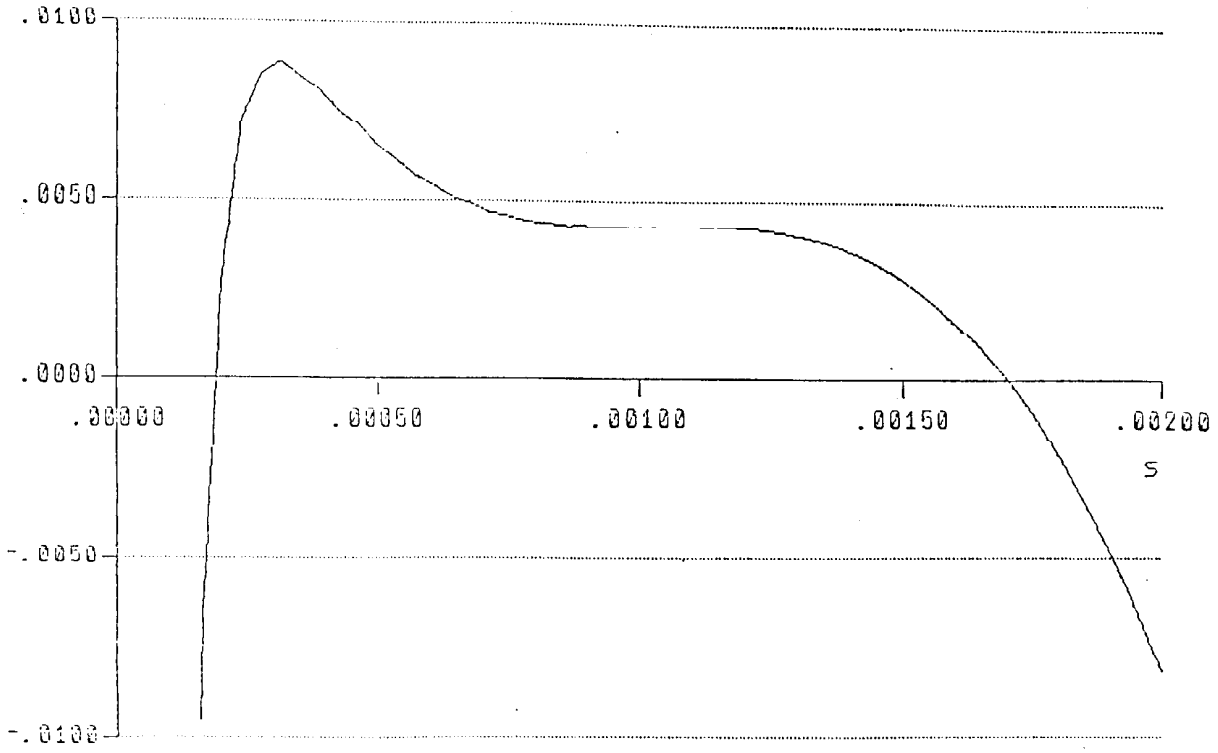

Figure 15. B-Modulator Optimum Circuit, Output Voltage U_ℓ. Figured: $\left(\frac{U_\ell}{10000\ V} - 1\right)$ vs. Time

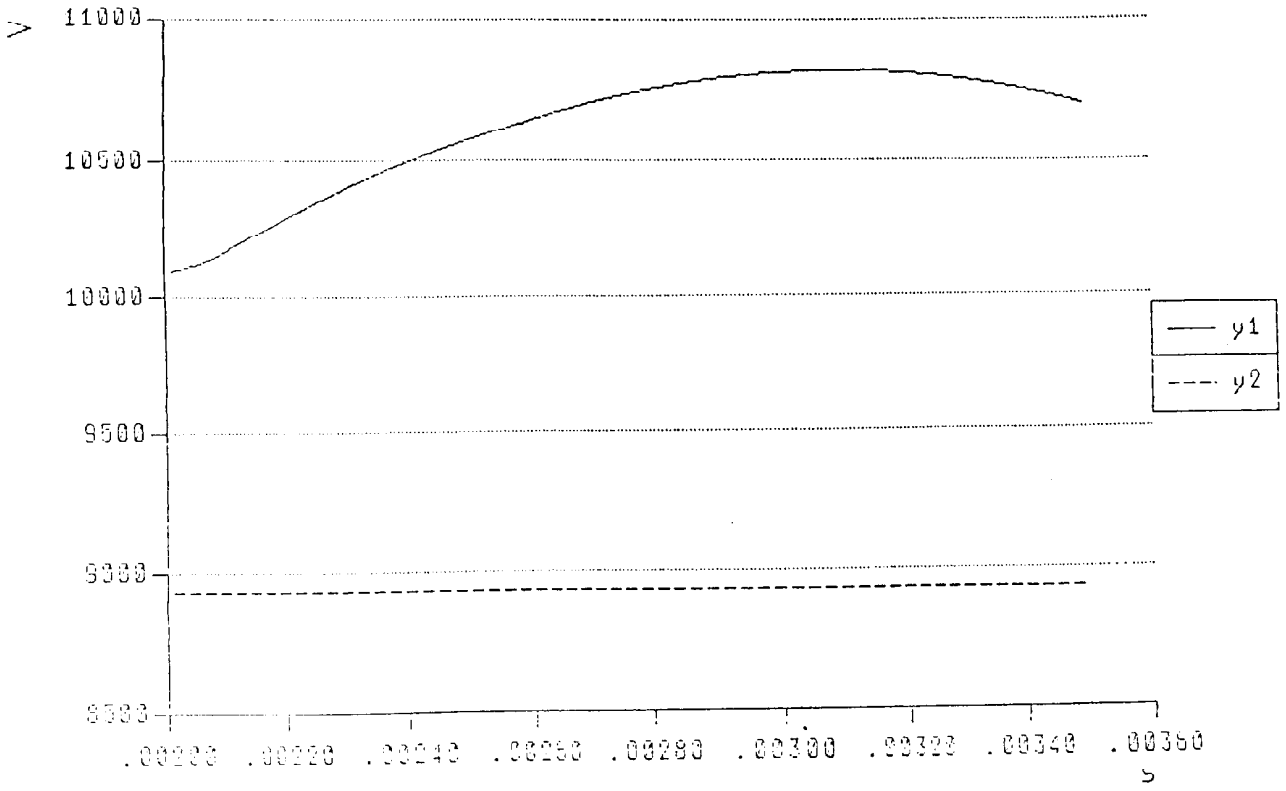

Figure 16. B-Modulator, Optimum circuit, no Recharge.
y1: Forward Off-State Voltage of the Semiconductor Switch, y2: Main Capacitor Voltage.

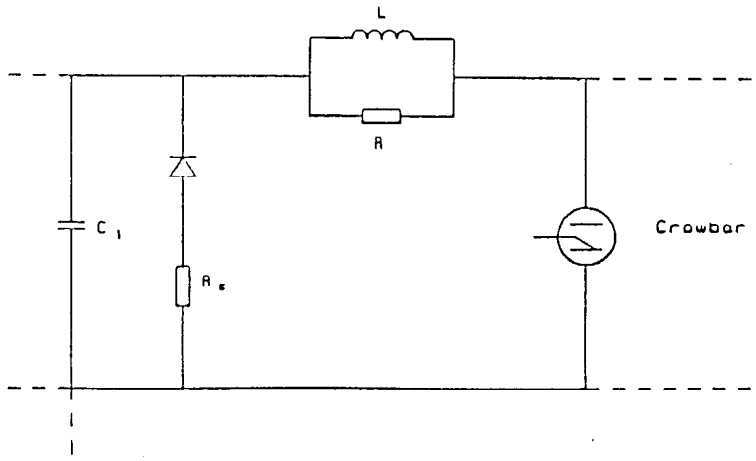

Figure 17. B-Modulator. Main Capacitor C_1. Crowbar and Short Circuit-Dump.

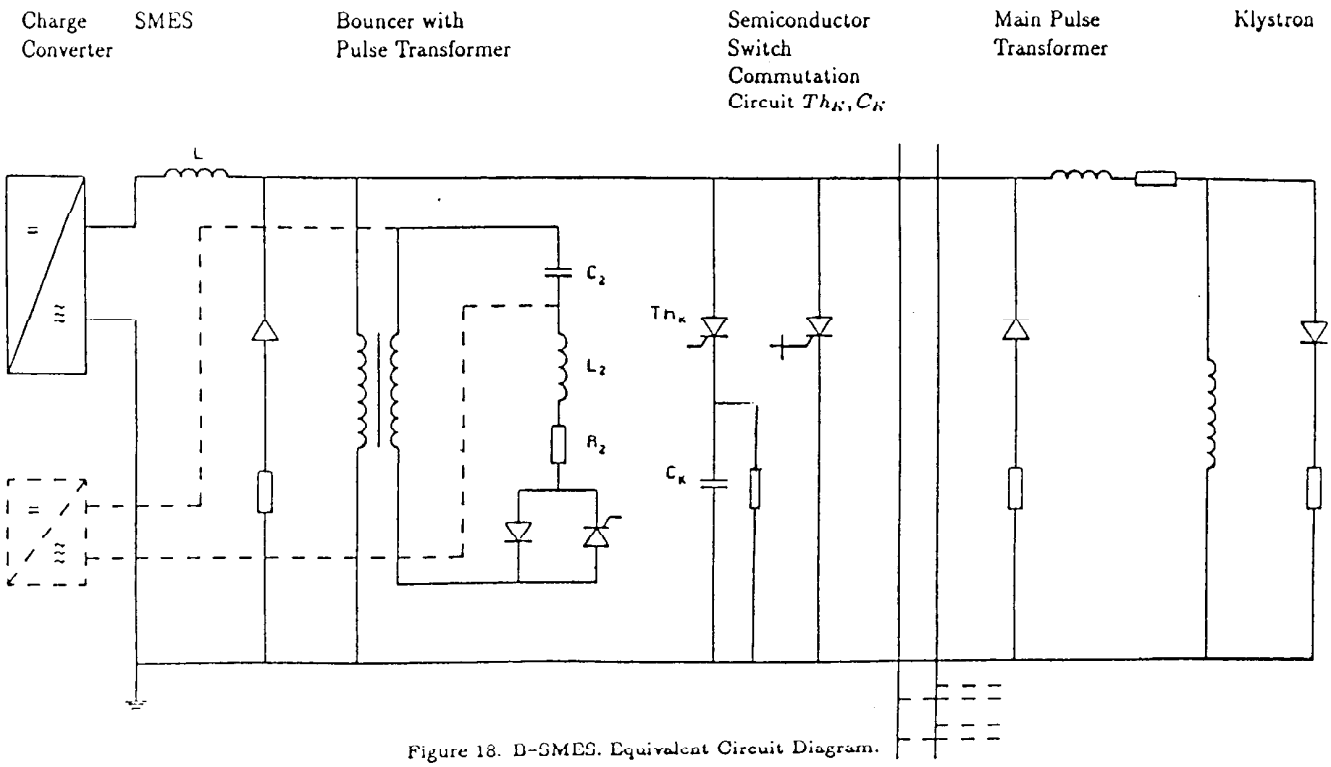

Figure 18. B-SMES. Equivalent Circuit Diagram.

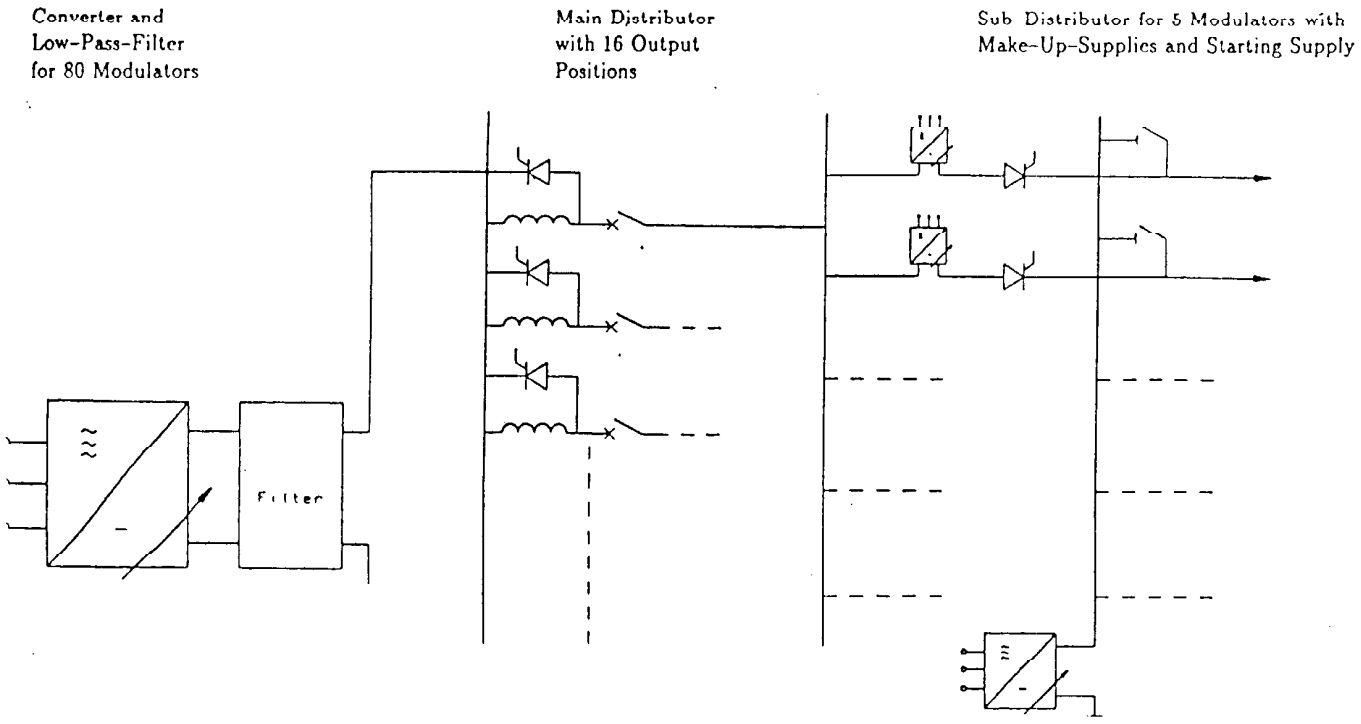

Figure 19. Common Charge for 80 Modulators. Principle Circuit Diagram.

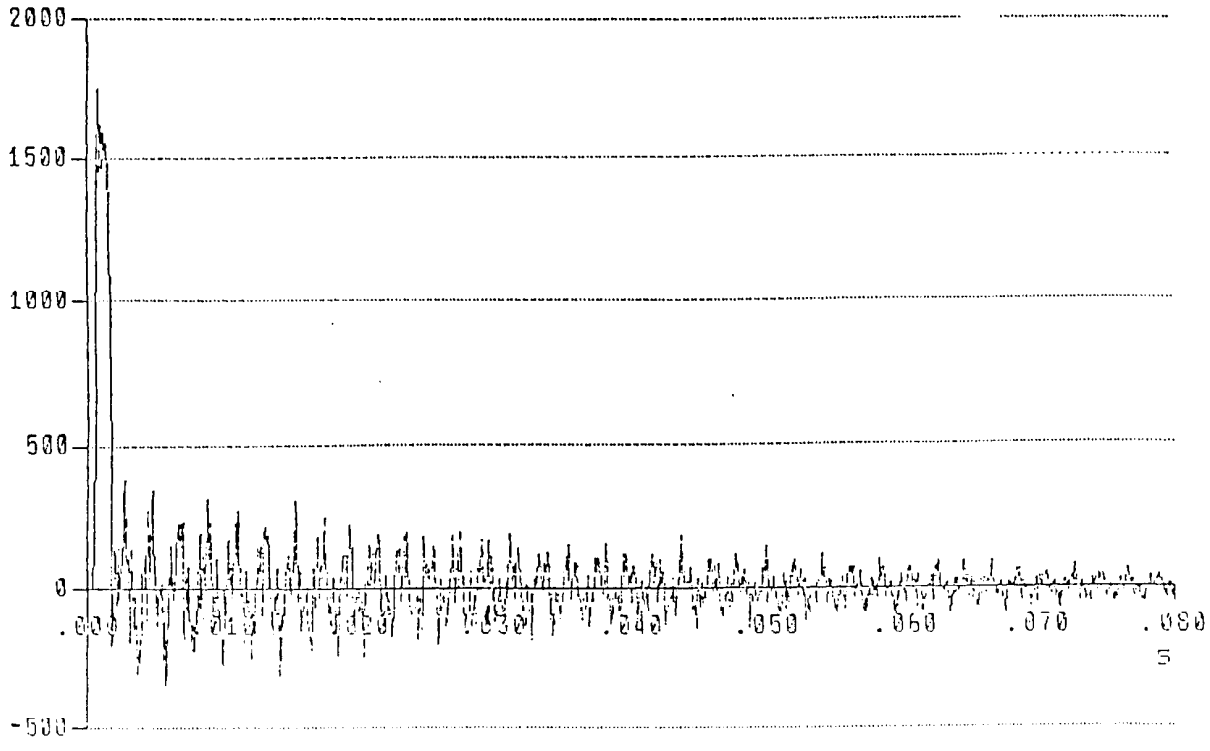

Figure 20. Mismatched Ladder Network, $\alpha = 0.4$. Inductor Current, Middle Position. No Recharge.

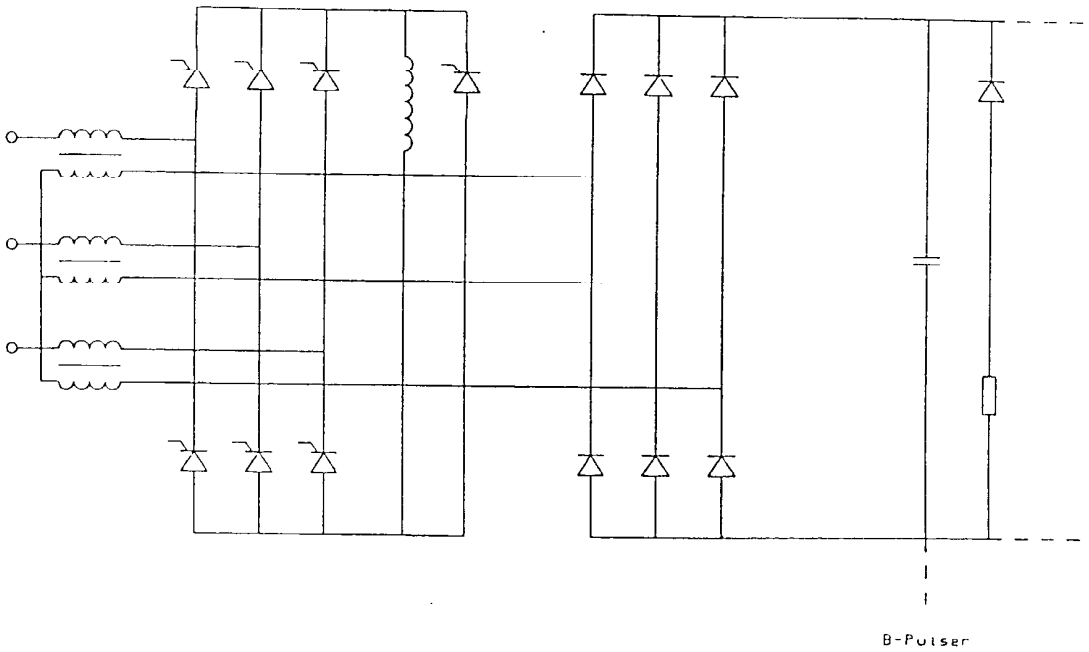

Figure 21. Single Charge of B–Modulator Main Capacitors. Converter Principle Circuit Diagram.