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FPGA Based, DSP Integrated, 8-Channel SIMCON, ver. 3.0.

Initial Results for 8-Channel Algorithm

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Abstract

The paper describes design, construction and initial measurements of an eight channel electronic LLRF device predicted for building of the control system for the VUV-FEL accelerator at DESY (Hamburg). The device, referred in the paper to as the SIMCON 3.0 (from the SC cavity simulator and controller) consists of a 16 layer, VME size, PCB, a large FPGA chip (VirtexII-4000 by Xilinx), eight fast ADCs and four DACs (by Analog Devices). To our knowledge, the proposed device is the first of this kind for the accelerator technology in which there was achieved (the FPGA based) DSP latency below 200 ns. With the optimized data transmission system, the overall LLRF system latency can be as low as 500 ns. The SIMCON 3.0 sub-system was applied for initial tests with the ACC1 module of the VUV FEL accelerator (eight channels) and with the CHECHIA test stand (single channel), both at the DESY. The promising results with the SIMCON 3.0. encouraged us to enter the design of SIMCON 3.1. possessing 10 measurement and control channels and some additional features to be reported in the next technical note. SIMCON 3.0. is a modular solution, while SIMCON 3.1. will be an integrated board of the all-in-one type. Two design approaches - modular and all-in-one, after branching off in this version of the Simcon, will be continued.

Keywords: Super conducting cavity, cold option, cavity simulator, multi channels cavity controller, linear accelerators, FPGA, FPGA-DSP enhanced, VHDL, FEL, TESLA, TTF, UV-FEL, Xilinx, FPGA based systems, LLRF control system of third generation, electronics for UV-FEL, X-Ray FEL and TESLA.

SIMCON, ver. 3.0.

CONTENTS

1 Introduction

This work is a continuation of the efforts on the SIMCON series of devices, which started a novel generation of FPGA/DSP/OPTO/EMBEDDED-PC based LLRF control system for a superconducting cavity.

This paper describes an electronic module of SIMCON 3.0. The device was designed as a semi-standalone component of the LLRF control system for a single CRYOMODULE section of the VUV-FEL accelerator in DESY. Each section (ACC-N, N=1,2,3,...6) contains 8 superconducting (SC) cavities, thus, the device features 8-channels. A general diagram of the control feedback loop of the LLRF system was presented in fig.1. This figure shows schematically the position of the SIMCON 3.0. inside the whole LLRF control system. The SIMCON 3.0 device was realized as a Daughter Board (DB) situated on the LLRF Mother Board (MB). The LLRF-MB was placed in the standard VME crate. The multi-channel cavity control and simulation algorithm was implemented in the FPGA chip.

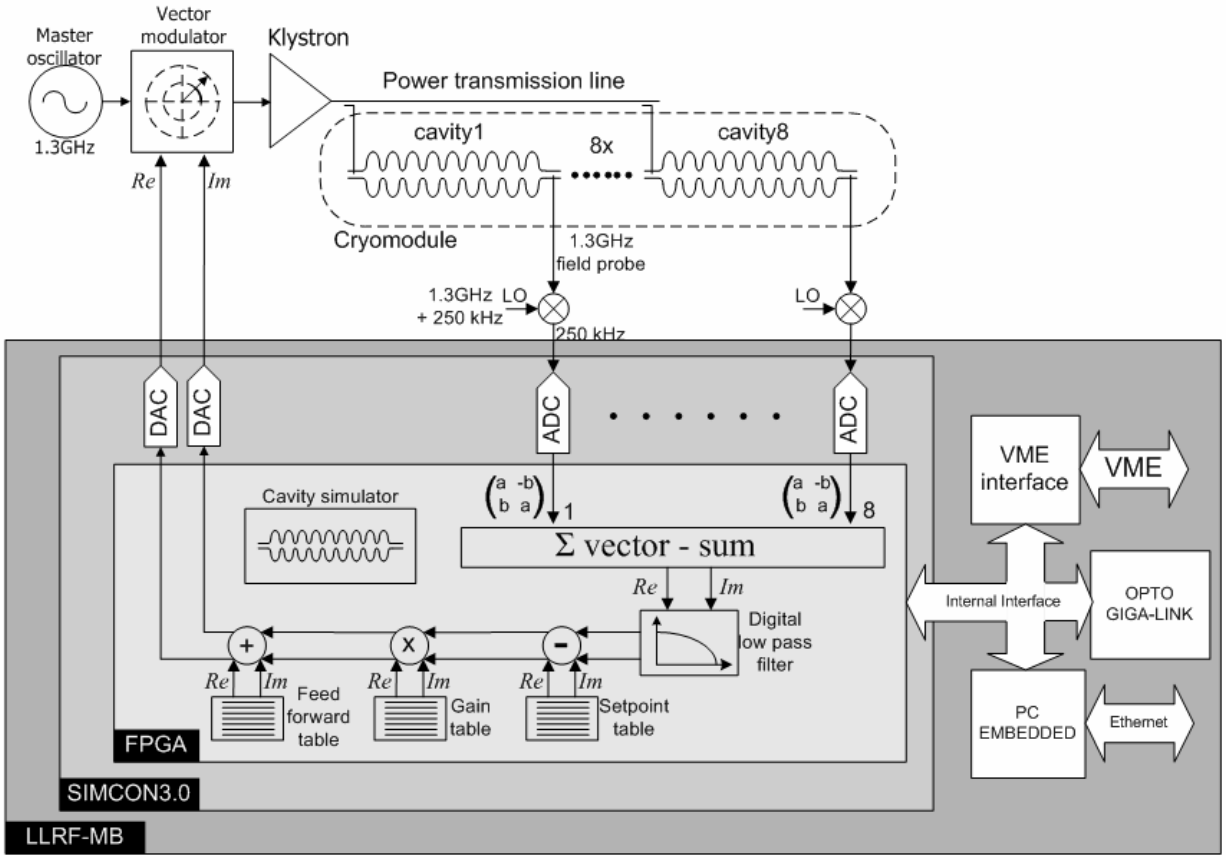

Fig. 1. A general diagram of the LLRF control system with the usage of the SIMCON 3.0 module.

The measurement signals, of 1.3GHz in frequency, are taken from the cavity outputs - *cavity1... cavity8*. These signals are downconverted in frequency to the intermediate value of 250kHz in multichannel dovnconverter circuits. In the next step, they are directly forwarded to the analog inputs of the SIMCON 3.0. module. All the input channels possess nondependent

analog, isolating amplifiers and 12-bit ADCs (ADC1…ADC8) [9]. The ADCs are directly coupled to the FPGA VirtexII-4000 chip [13].

The digital I/Q (in-phase and quadrature) signals, obtained from the AD converters, are fed into the input block of the numerical control algorithm. The algorithm bases on the programmable DSP functional blocks embedded in the FPGA Virtex II chip. There were used fast, 18x18 bit, multiplication and summation circuits, realized in the programmable logic [1,2]. The result of the algorithm are digital *Re* and *Im* signals. These signals are used to control the amplitude and phase of the EM field in the SC cavities. These signals undergo a conversion in the DAC1 and DAC2 [12] and, as analog ones, are input to the vector modulator.

The *SIMCON 3.0* module has implemented a digital algorithm of the cavity simulator [2]. The algorithm, in this version, has the ability to control eight input channels. It can work autonomously with the module for the test, training and teaching purposes.

The *SIMCON 3.0* module was designed as a user's mother bard (mezzanine card) to cooperate with a mother bard of the LLRF control system [3]. The LLRF-MB is an autonomous and standalone 6HE device, able to work in the EURO crate. The *SIMCON 3.0* has the following features:

- Standardized communication system with the VME-bus [8]
- Control via the Embedded PC processor and via the Ethernet 100TP [7],
- Remote configuration of the FPGA chip via the standardized JTAG interface [9],
- Fast, electrical data transmission buses, capable to realize connections with other daughter modules, like the OPTO module [4]. The latter provides the transmission rate up to 1,6Gbps now and up to 10Gbps in the near future,
- Distribution of common clock and synchronization signals, enabling synchronous work of several daughter module on a single LLRF-MB hardware platform,
- Provides all required levels of power supply and voltages.

The design of the *SIMCON 3.0* module takes into account the near-term development of the system. The board is ready for the usage in the LLRF control system, the RF-Gun control system, and can work with the predicted Intermediate Frequency (IF) of 81 MHz. The analog input and output channels may work in the bandwidth not less than 100 MHz. The applied ADCs and DACs have sampling frequencies bigger than 100 MHz.

2 Structure of control module for the X-FEL accelerator

The *SIMCON 3.0* module was realized as an integrated electronic block. It possesses all necessary components for the control of a single section (crio-module) of the VUV-FEL accelerator. The basic block diagram of the module was presented in fig. 2.

The design assumptions for the *SIMCON 3.0* module predicted a flexible cooperation with the frequency downconverter, for a considerable range of the IF values. The IF values were considered as 250 kHz, 81 MHz and other values, for the carrier frequency of 1,3 GHz. Other features of the SIMCON 3.0 design are: fast DSP processing – of the latency lower than 500 ns, modular construction, programmable configuration, monitoring and data acquisition capabilities.

The following design assumptions were implemented:

- Eight input analog channels:
  - Each channel was equipped in nondependent ADCs of 14 bits resolution,
  - Sampling frequency of the converter is in the range of 50 – 100 Msps (there is a possibility for a fast, hardware based, averaging of the I/Q vector,
  - The input voltage range is ±1V/50Ω,
  - There is applied an isolating amplifier, with symmetric output, to minimize the SNR value.

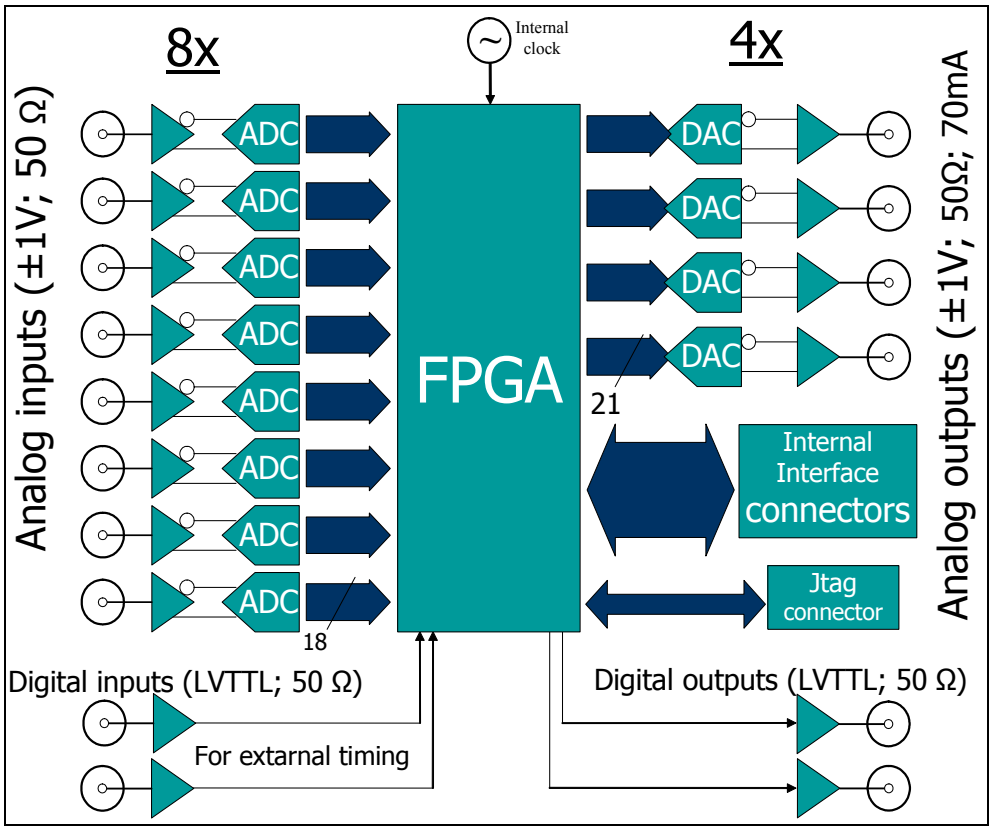

Fig. 2. Functional block diagram of the SIMCON 3.0 control module

- Four output analog channels:
  - Each channel is equipped with a DAC of 14 bits resolution and symmetric output to minimize the SNR,
  - The converter frequency is in the range 40 – 160 Msps (the converter realizes additionally a hardware approximation of the signal),
  - The output voltage range is ±1V/50Ω,
  - There is applied an isolating amplifier of the voltage range ±1V/50Ω.

- Two input and two output, buffered, digital channels, of the LVTTL standard, used for the input and output of synchronization signals.

The further part of this chapter characterizes the most important electronic blocks of the LLRF processing channel, which were used for the construction of the *SIMCON 3.0* module.

2.1 Analog – digital input Channel

Each of the eight input channels consists of an analog buffering circuit for the input signal and with an ADC chip. An input antialiasing filter was intentionally omitted, here in he design, due to the necessity to work with the large oversampling.

The external, asymmetric analog signals are input to the MCX type of socket. The wave impedance is 50Ω. The sockets are wideband and provide good impedance matching.

Each of the channels has a separate, full-differential, integrated amplifier, AD8138 by the Analog Devices. It was configured as a buffer with the unity of amplification (GAIN=1). It changes the asymmetric input signal to the differential signal. The differential signal is input directly to the ADC.

The ADCs are fast, 14-bit, AD6645 chips by Analog Devices [9]. These converters provide the maximum sampling frequency up to 105 Msps. The analog input bandwidth is 270 MHz. The SIMCON 3.0 module is able to work with the downconverted signal of IF=81 MHz and of bigger frequency.

There was used a differential analog input. It is less susceptible to the EMI. The internal construction of the converter assures a physical separation of the digital part and analog part of the system. This results in the SNR of 75 dB. The converter has an internal reference voltage source and the system of S&H (sample and hold).

2.1.1 Power dissipation in ADCs

The catalog data for the ADC chip AD6645 is 1,5 – 1,75 Watt of power dissipation during the nominal work conditions. A laboratory experiment was designed to try to overheat the chip above the nominal working temperature. The catalog data was used and the relation from [6]. The catalog data give information of the accumulated thermal resistance Θ_{JA} , which is a sum of the thermal resistances between the junction and the package, the package and the ambient space. This resistance depends on the work conditions of the chip. The calculations assume the most critical work conditions, at which Θ_{JA} = 30 ^{o}C/W and the ambient temperature is 30 ^{o}C. Then, a simplified relation for the chip temperature is:

$$T_J = T_A + \Theta_{JA} * P \tag{1}$$

It means, that the chip temperature may reach the maximum value equal to:

$$T_J = 30^o C + 30^o C / W * 1{,}75W \cong 83^o C \tag{2}$$

It is a temperature close to the maximum allowed value of 85^{o}C. Miniature metal radiators were glued to the upper surface of the converters to provide additional cooling.

2.2 Digital – analog output Channel

The four output digital – analog channels use 14-bit, DACs AD9772A [12]. The converter provides maximum work frequency of 160 Msps. The chip has a configurable filter of the second order (low-pass or high-pass) and a differential analog output.

The differential signal, after ADC, is input to the amplifier chip Max4444 of the amplification coefficient GAIN = 2. This chip converts the signal from the differential format to the asymmetric one. The output from the SIMCON 3.0 is via the MCX sockets of 50Ω resistance.

2.2.1 R_{set} resistor value of DAC

According to the catalog data of ADC AD9772, it is required that the R_{set} resistor is determined. This resistor controls the reference current *Iref*. This ADC has the current outputs, which may work in the range from zero to a pre-set maximum value. The maximum value is in the range of 2 – 20 mA.

It stems from the catalog data, that the converter has the biggest work accuracy at the maximum value of the output current $I_{OUT} = 20mA$. The maximum potential between the current outputs and the ground is $500mV$. Thus, the load resistance R_{out} should be:

$$\frac{500mV}{20mA} = 25\Omega \tag{3}$$

In order to add a margin of safety, the resistors were taken of 50Ω. This gives the maximum values of the current $I_{OUT} = 10mA$. This current, divided by 32, determines the reference current, which equals: $Iref = 312.5\mu A$.
The value of R_{set} resistor, calculated as a ratio of the reference voltage (of constant value 1,2V) to the reference current:

$$R_{set} = \frac{V_{ref}}{I_{ref}} = 3840\Omega \tag{4}$$

In order to obtain the required range for the DAC, the R_{set} resistor should be chosen very precisely.

2.3 Distribution of clock signal

The module of SIMCON 3.0 may use one of two alternative sources of the clock signal:

- Oscillator of 60MHz, directly connected to the FPGA chip,
- External clock, forwarded to one of the digital inputs.

The FPGA matrix re-distributes the clock signal between the remaining components of the board. This situation was schematically presented in fig. 3. A nonsymmetrical source of the clock signal is converted, inside the FPGA, to the differential signals of the PECL standard. These signals are individually distributed to all the ADCs and DACs.

The VirtexII-4000 FPGA chip has 12 complex PLL blocks. These were used as multipliers, dividers and phase synchronizers of the clock signal. The inbuilt DCM (digital

clock manager) components allow to obtain the clock signal of a broad range of frequencies from 1.5 MHz to 270 MHz.

2.4 Digital Inputs and Outputs of SIMCON 3.0.

The module of *SIMCON* 3.0 was equipped in two LVTTL (3,3 V) inputs and two digital outputs. All signals are using the MCX connectors of the wave impedance 50Ω. The signals are properly buffered with the usage of single logical gates of the chip 74LVT2245.

Additionally, the board of the module has an 8-bit input/output port of a general usage. The port is directly connected to the FPGA chip. It is devoted to conduct the initial tests and hardware monitoring.

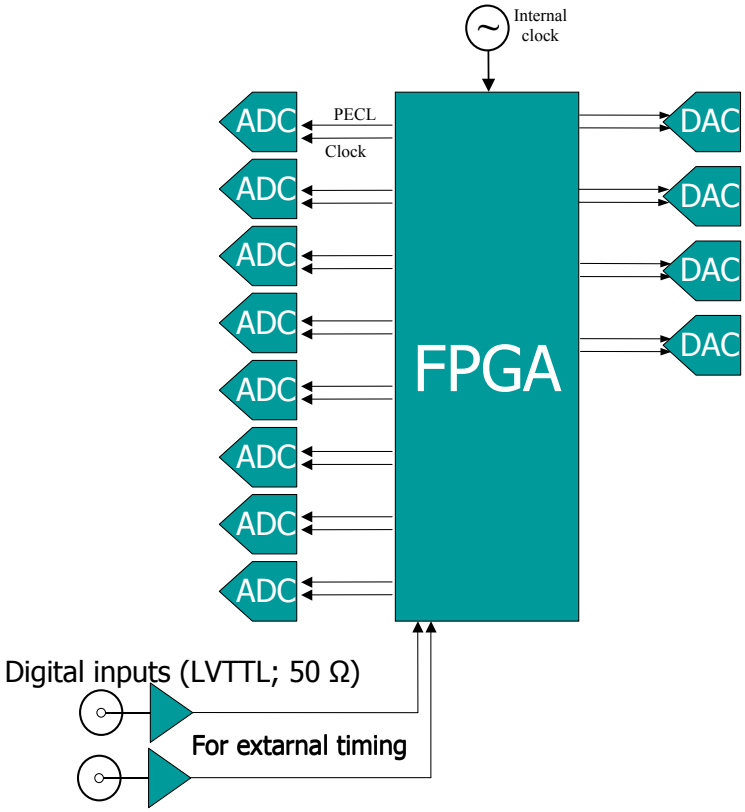

Fig. 3. Block diagram of clock signal distribution.

2.5 Communication and Configuration of SIMCON 3.0 module from the level of the LLRF MB

The communications between the upper level of the supervisory computer system and the *SIMCON 3*.0 module is done via the proprietary *Internal Interface* [3] bus. The controller of the bus is embedded in the LLRF-MB platform. The controller gives access to a 32-bit address

space for a 32-bit data word. The PCB of *SIMCON 3.0* may transfer up to eight nondependent asynchronous interrupts.

The configuration of the FPGA chip is realized by the JTAG controller. The JTAG controller is present on the LLRF-MB. It gives access to the individual JTAG chains for the particular user boards. Thus, the loading process of the FPGA does not require other components in the JTAG chain. The programmable control of the JTAG interface may be done from the level of the VME, as well as from the PC_EMBEDDED block.

2.6 FPGA chip with embedded DSP components

To realize fast, hardware based DSP calculations, the following FPGA chip was used - VirtexII - XC2V4000 by Xilinx [13]. The matrix contains the following components, blocks and features:

- 4 MIL of logical cells (LCELL) used to realize the control blocks, data acquisition, data processing, etc.,
- 120 fast, hardware multiplication blocks of 18x18-bits. These blocks are the basis for realization of the cavity control algorithm. The addition and subtraction operations are realized in the programmable logic circuitry,
- 2Mb of configurable RAM memory was implemented as tables for variable parameters of the DSP algorithm and as data buffers,
- 12 PLL blocks provide the possibility of precise phasing of the clock signals for the converters, for digital inputs and for the internal logics. The internal distribution system for the clock signal works with the maximum speed of 420 MHz.
- 1152 pin package, fine-pitch BGA, featuring 824 configurable I/O pins to be programmed by the user. This large number of pins allows for convenient connection of all external but integrated circuits. This number of peripheral devices (positioned on the LLRF-MB) grows essentially with the users' demand. For the purpose of very fast, small distance communications, there were used the digital standards like symmetrical transmission strip lines LVDS (*Low-Voltage Differential Signaling*) and LVPECL (*Low-Voltage Positive Emitter-Coupled Logic*).
- JTAG- IEEE 1532 (*Boundary-scan*) interface, predicted for the hardware configuration.

3 Realization of SIMCON 3.0 control module as a DB

The dimensions of the designed and realized PCB are 162mm x 142mm. It was realized as a daughter board on the LLRF [3] MB platform. The module uses two user slots and is connected with the MB by four miniature linear connectors.

Figure 4 presents a photograph of the upper side of the SIMCON 3.0 PCB. The signal connectors for the LLRF processing channel are described. All the discrete components, connectors, converters and amplifiers are positioned from one side, to facilitate the access with a broadband measurement probe. There were used a precise series of the broadband MCX connectors. These sockets have the bandwidth of up to several GHz and subminiature dimensions. These dimensions are of extreme importance, because the SIMCON DB is small, and there are 12 inputs for analog signals for a single side of the PCB.

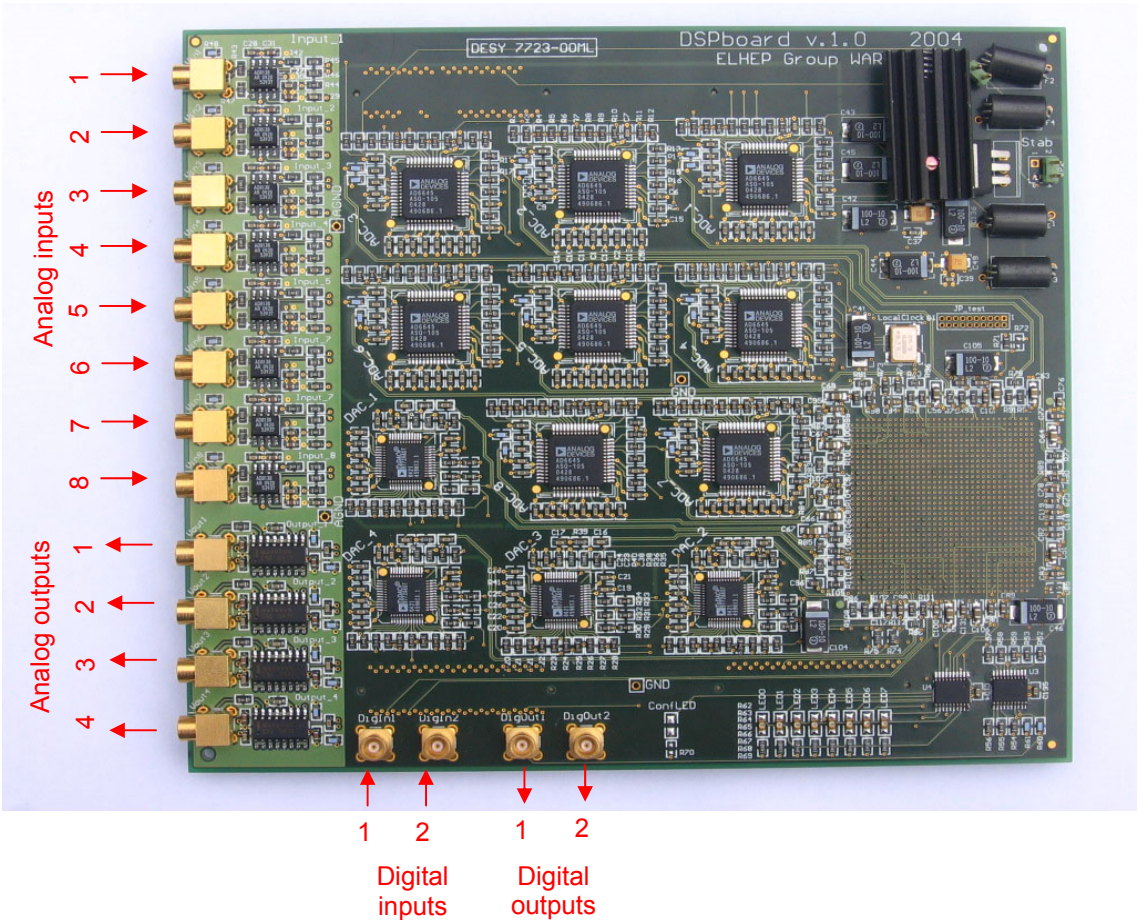

Fig. 4. Upper side of the *SIMCON 3.0* module PCB

The PCB features 4 additional digital sockets for the distribution of synchronizing signals from the LLRF system. The board has eight LEDs and an eight-bit port controlled directly from the FPGA. They serve to monitor the work of FPGA chip.

Figure 5 presents the bottom side of the SIMCON 3.0 PCB. There are visible four linear connectors for embedding of the DB sub-system on the LLRF-MB. The communication is provided via these connectors with the supervising upper layer control system, and with the FPGA configuration via the JTAG standard, as well as the supply source for the FPGA chip. The back-side features the FPGA chip with its fine-pitch BGA package. The pins (soldering balls), in such a package, are distributed all over the chip footprint area, creating a regular matrix of connecting pads. The essential footprint of the package has small soldering pads connected with a matrix of vias. The vias give direct access to all pins of the FPGA on the other side of the PCB, as in seen in fig.5.

The SIMCON 3.0 PCB was made on the standard FR4 laminate. Figure 6 presents a cross section of the PCB (*layer stack*). It consists of 16 layers: four negative power supply layers, and twelve signal layers.

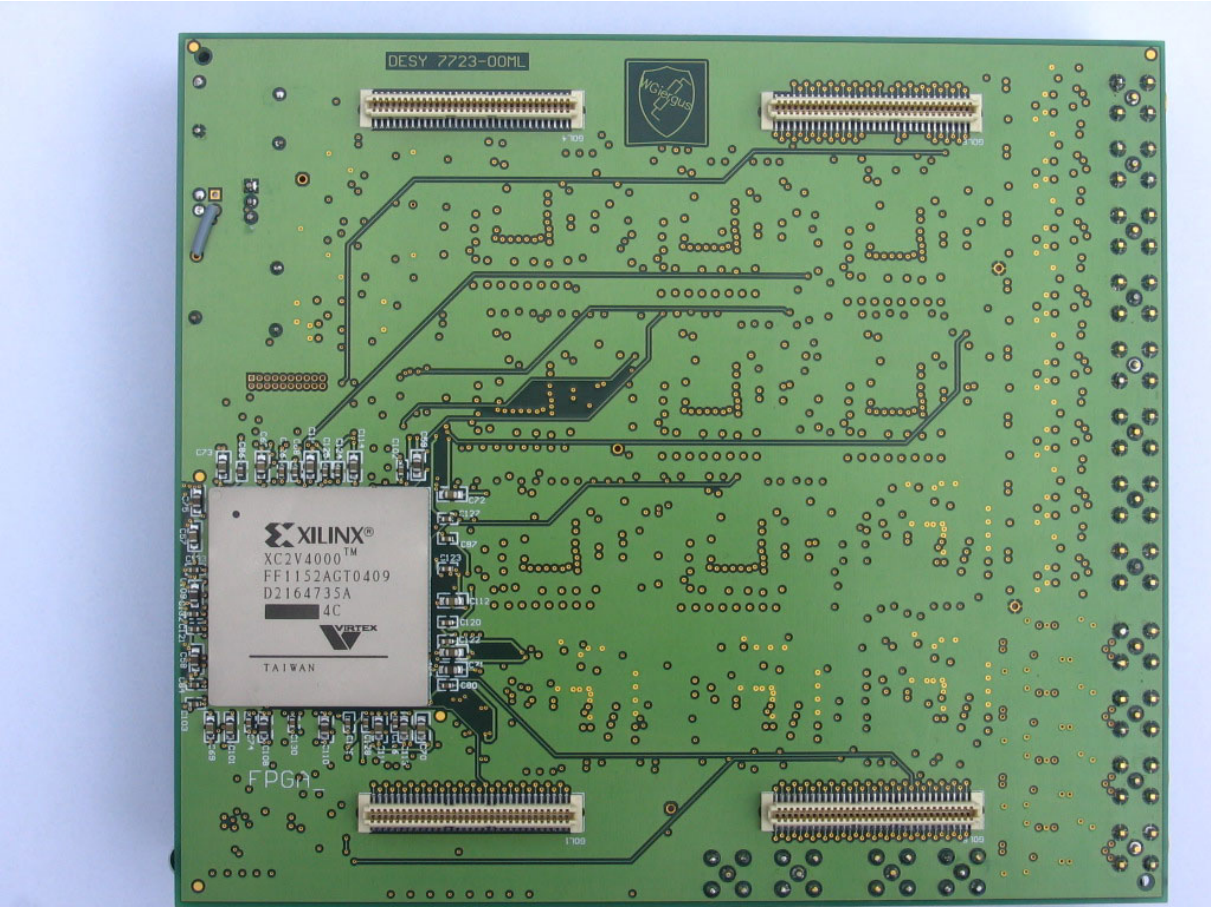

Fig. 5. Bottom side of the SIMCON 3.0 PCB

The power supply layers feature three voltages for the analog part of the system (-5V; +5V; +3.3V), three voltages for the digital part of the PCB system (+1.5V; 3.3V; +5V), and separate analog and digital chassis. The analog part was separated from the digital with the aid of choking coils of 45µH.

The first layer (i.e. *Top layer*) contains the most critical (against the frequency demands and the stability of impedance) signal paths. These are the differential paths of analog signals from the ADCs and to DACs converters and differential paths for digital clock signals (in LVPECL standard). The next layer is a chassis. The PCB has more than 300 decoupling capacitors. The kinds and number of capacitors stem from the requirements included in the technical specifications of the particular chips. The most critical requirements concern the FPGA Virtex II chip [9] and decoupling of analog channels. After the SIMCON 3.0 module was fabricated, debugged and powered on, there were performed several measurements of the system. The most important parameters were checked. The results are shown synthetically in the next chapter.

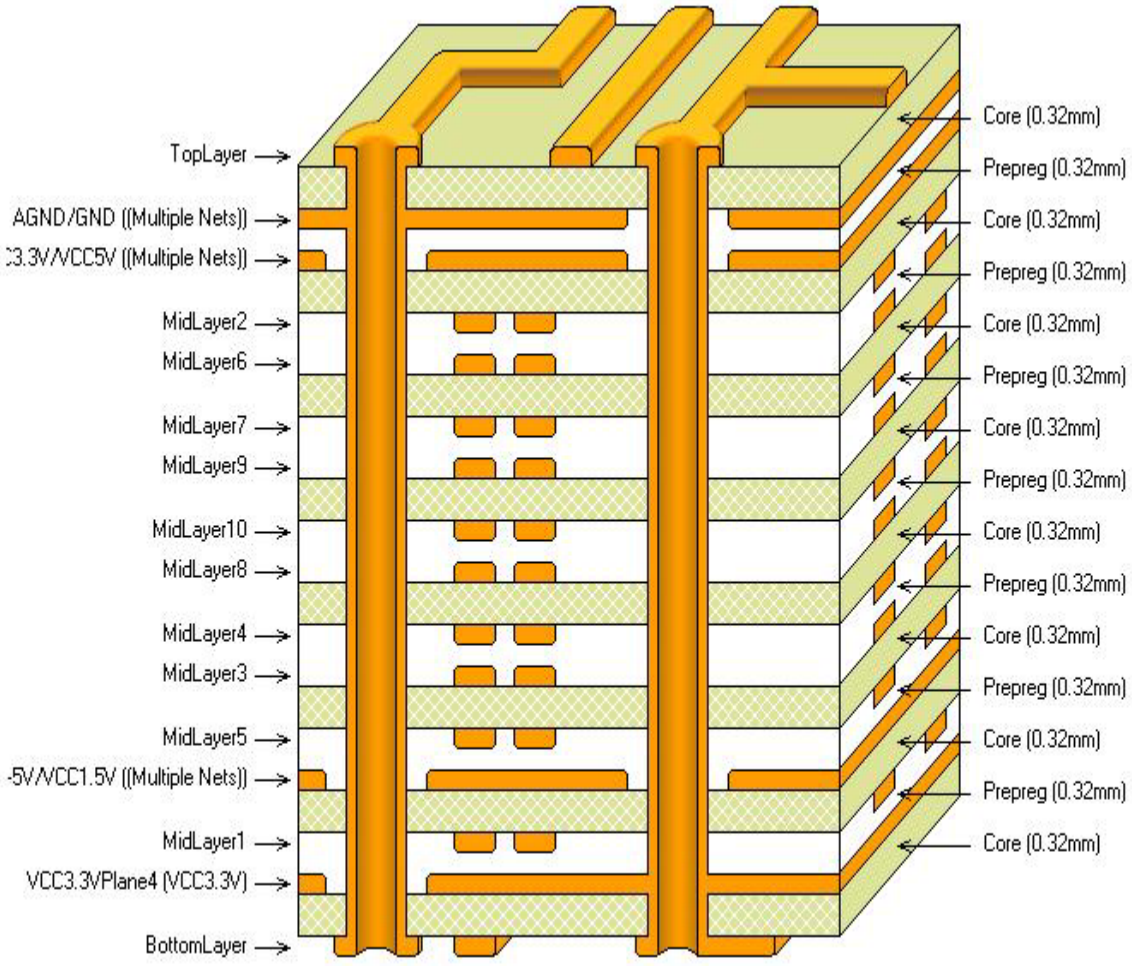

Fig. 6. Cross section via all layers of the SIMCON 3.0 PCB (layer stack)

4 Measurements of SIMCON 3.0. parameters and algorithm tests for LLRF system

The measurement were done with the aid of the *Wave Runner* oscilloscope by LeCroy of the analog bandwidth 1GHz and the maximum sampling frequency 10 Gsps. The bandwidth of used probes was 500 MHz.

1. The measurement results of the real value ranges of analog signals were presented in fig. 7 and table 1.

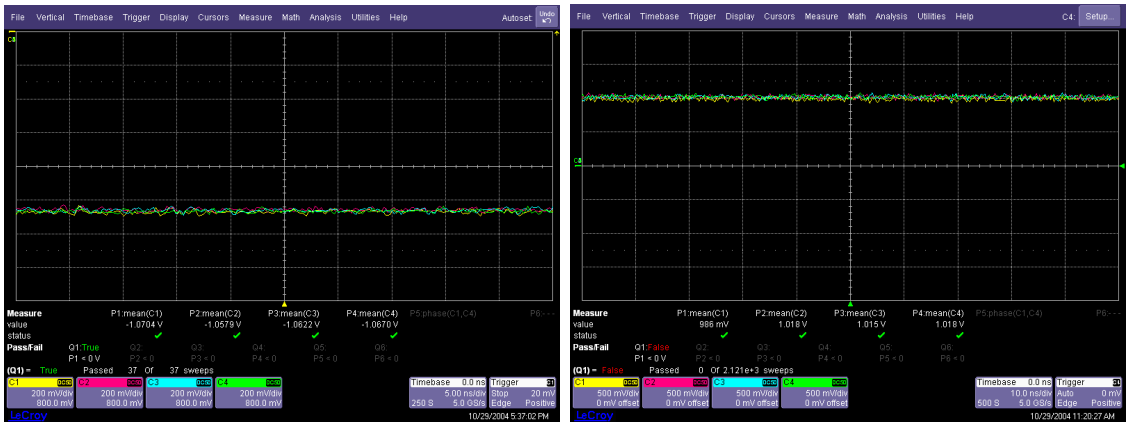

Fig. 8. Measured voltage levels on the outputs of PCB

kanał	Minimum	Maksimum	Offset [mv}
1	-1.14	1.05	-39
2	-1.11	1.07	-26
3	-1.12	1.1	-25
4	-1.11	1.07	-32

Table 1.

2. The measurement of a single bit quality input to the ADC chip was presented in fig. 8. The oscilloscope image shows the quality of bits arriving at the input circuit of the converter. There were obtained smooth edges of the signal, minimizing the level of reflections, by a proper choice of the passive components for the transmission channel.

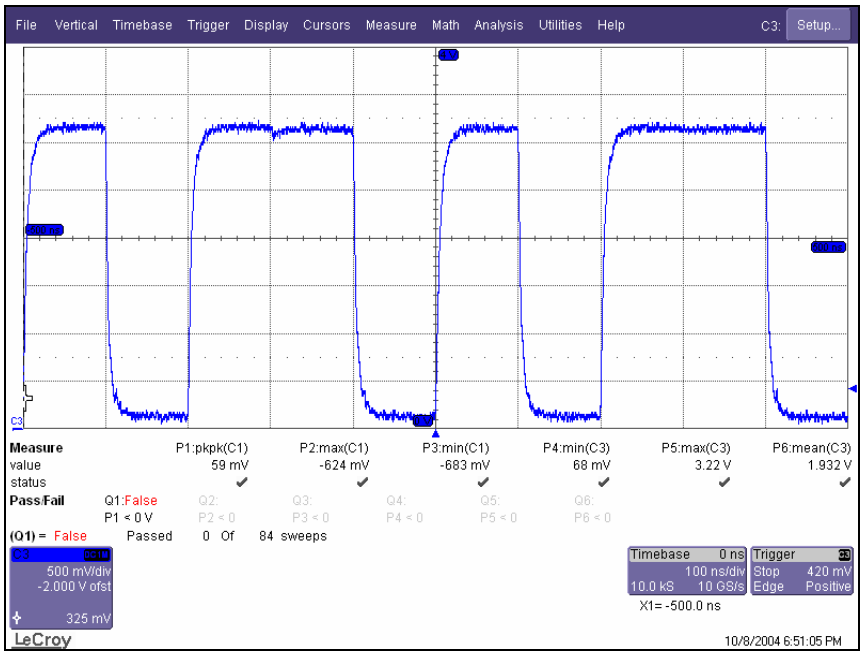

Fig. 9. Input signal on a single, the most representative channel of the ADC

3. There was measured the quality of differential signal. Fig. 10 presents a differential signal entering the ADC chip. The left panel shows the differential signal prepared in the FPGA chip by a simple negation of one of the signals. The right panel shows a clock signal obtained after using the LVPECL block present in the Virtex II chip.

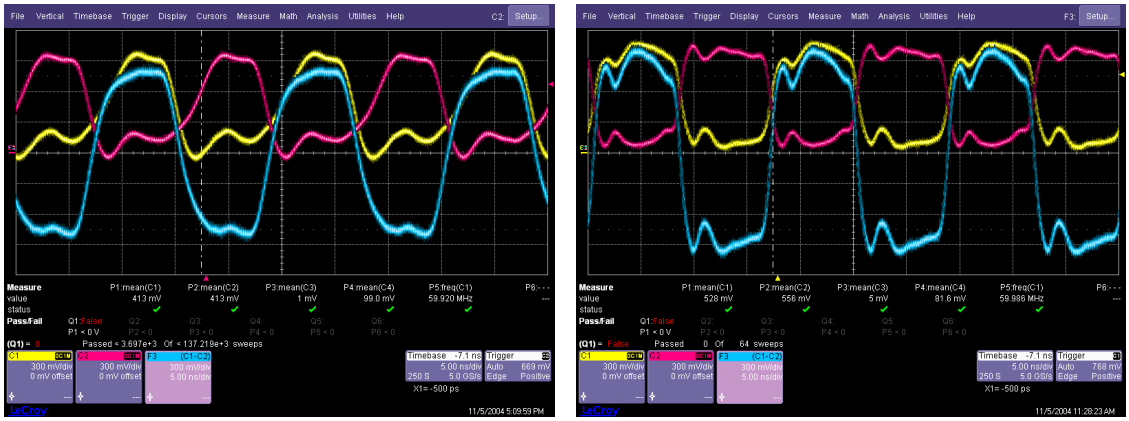

Fig. 11. Differential signal of the 60 MHz clock

4. The latency was measured along the path from the sample taking point (at the input of the module) to the sample exit point (at the output of the device). The measurements were made for the following data: ADC rate of sampling was 80Msps, DAC rate of sampling was 160Msps. The above rates were obtained via the inbuilt PLL circuits. The input signal was a single and short pulse.

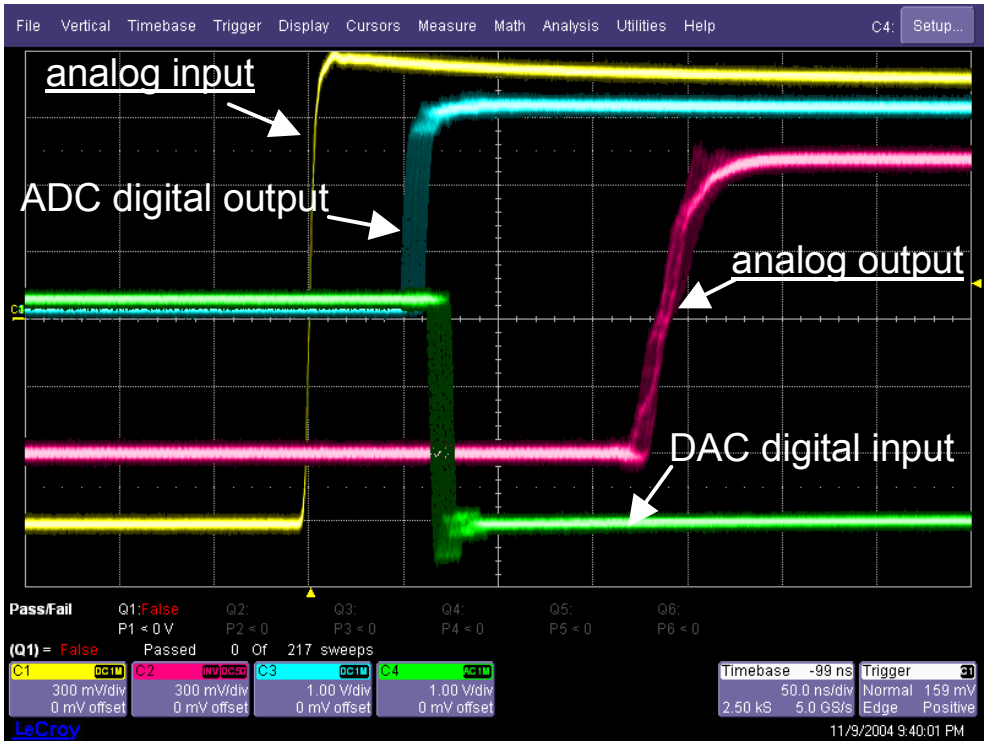

Fig. 12. Latency measurements for ADC3 - 80 MSPS and DAC1 -160 MSPS).

Figure 12 presents an exemplary oscilloscope image from the partial measurements of the total control loop latency. This latency is 190 ns for the investigated board. The signal blurriness/fuzziness stems from the sampling effect with a clock signal not synchronized with the input signal.

The measured latency for particular parts of the LLRF processing channel was presented in figure 13. The propagation time in the FPGA chip does not reflect upon a real latency input by the DSP algorithm, but only on the transfer time of the signals.

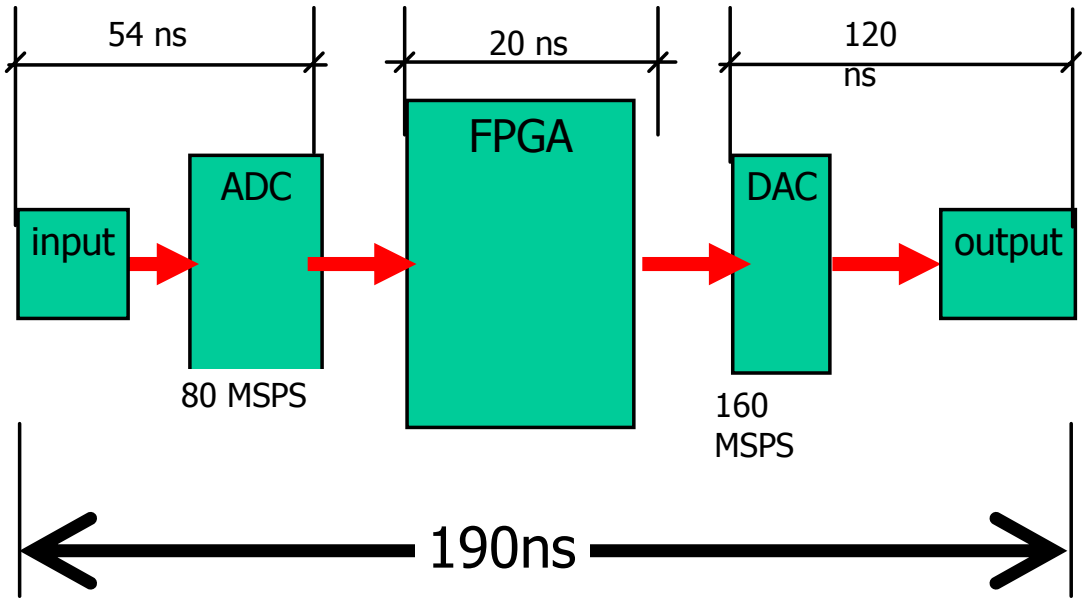

Fig. 14. Measured components of the latency for the LLRF signal processing channel

5. Fig. 15 presents the delay on the way from the analog input to the digital output from the AD6645 ADC. The oscilloscope image shows additionally the clock signal, in order to have a reference to the number of the clock periods, required for doing the conversion. According to the catalog data, the latency generated by the conversion process only, equals to 4 clock periods.

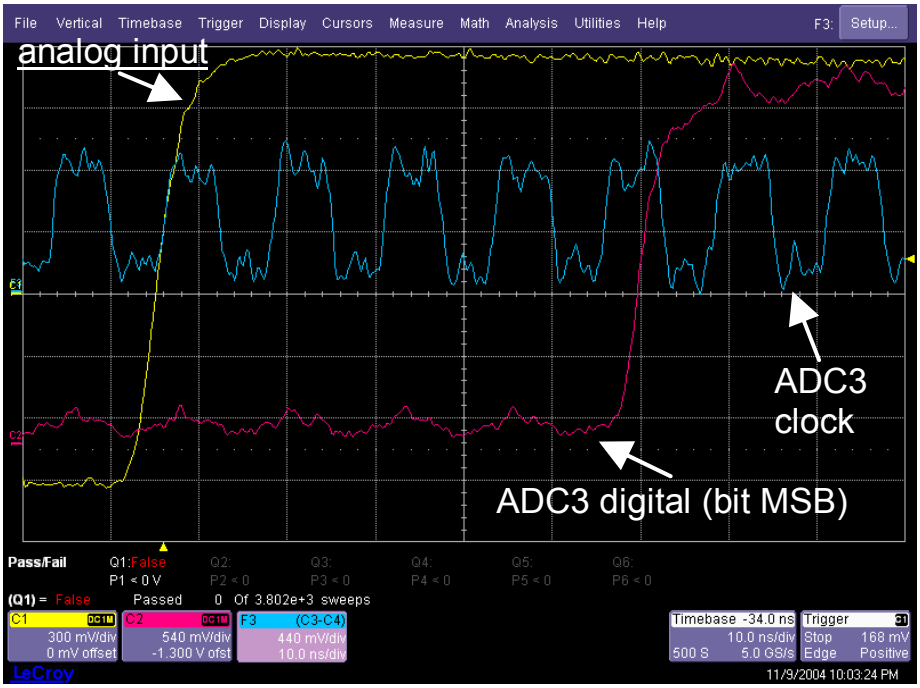

Fig. 15. Input signals to the ADC3 chip and the output latency for 80MHz.

6. Figure 16 presents the measurement results on the path from the DAC input to the analog output on the background of the clock signal. The conversion latency was 20 clock periods. The latency generated by the DAC is considerable. Thus, the timing of the converter with a multiplied signal of the basic clock is highly justified.

Fig. 16. DAC latency for 160Msps.

7. There was implemented a proper DSP algorithm for the control of the resonant SC cavity. The combined algorithm (including simulator and controller) was dedicated for the SC

linac of the XFEL/TESLA machine. The results are presented in fig. 17. The I and Q signals were visualized for the cavity simulator, which were extracted from the DACs outputs.

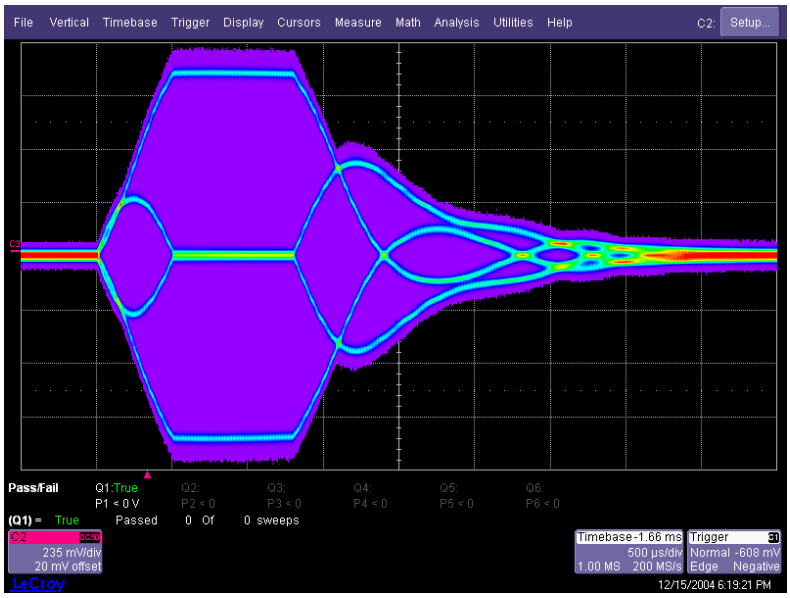

Fig. 17. SIMCON 3.0 measurement results: Control algorithm implementation with the cavity simulator

8. The noise signal was measured for the sampling frequency of 40 MHz. The measurement results enabled to determine the balance voltage shift and other basic noise parameter for particular channels.

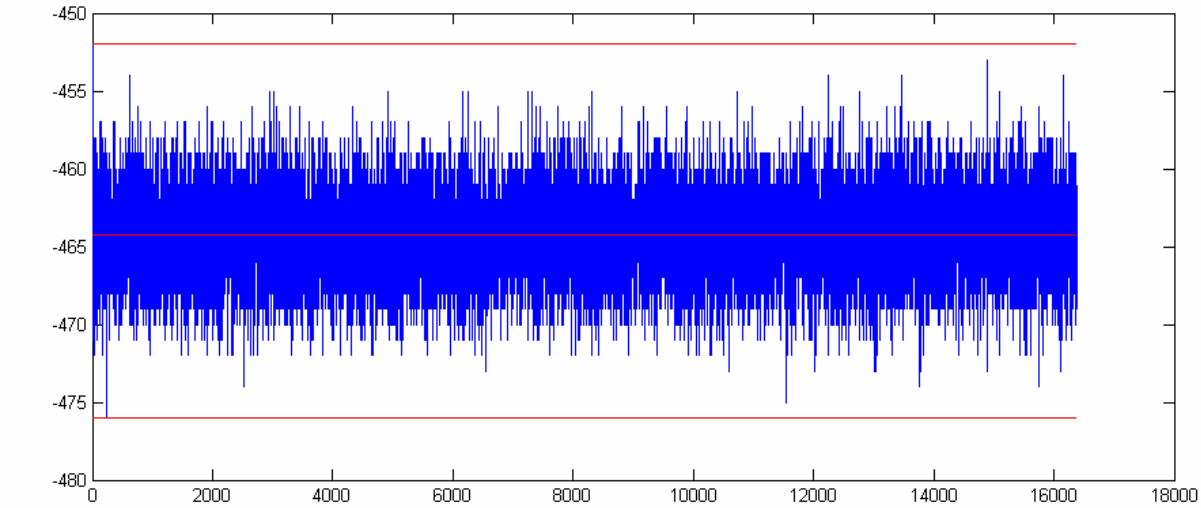

Fig. 18. Exemplary output signal on the ADC5 basing on the acquisition of 30 measurement series, each containing 16384 samples

9. Fig. 18 presents the result of data acquisition for a single measurement series of 16384 samples. The analysis was done for 30 consecutive series. The measurements were done for two different loads of the inputs: opened channel and loaded with a 50 ohm resistance.

a) The channel inputs are opened:

converter	average	minimum	maximum	σ	σ^2	offset [mV]
1	-514.6281	-525	-501	4.7371	22.4398	-73
2	-364.3429	-375	-349	3.8924	15.1507	-54
3	-386.9608	-397	-375	4.0354	16.2846	-55
4	-335.0779	-346	-323	2.8505	8.1254	-45
5	-463.3294	-476	-452	2.6947	7.2616	-63
6	-417.4330	-429	-405	4.0846	16.6839	-60
7	-412.8996	-425	-401	3.5761	12.7888	-57
8	-404.8848	-416	-394	3.1327	9.8139	-56

Table 2. Statistical parameters for particular channels for opened inputs

b)

c) The channel inputs are loaded with 50Ω resistance

converter	average	minimum	maximum	σ	σ^2	Offset [mV]
1	-120.8806	-134	-107	3.9707	15.7663	-17.34
2	27.3696	15	48	3.8148	14.5527	4.06
3	10.7092	0	22	4.0328	16.2638	1.53
4	78.3036	65	92	2.9632	8.7805	10.66
5	-55.9655	-66	-45	2.8101	7.8967	-7.71
6	-19.5990	-33	-7	4.1943	17.5922	-2.82
7	-7.5917	-19	4	3.6118	13.0449	-1.05
8	6.8433	-10	19	5.0231	25.2319	0.96

Table 3. Statistical parameters for particular channels for loaded inputs

5 Integration of SIMCON 3.0. with ACC1 accelerator module and CHECHIA test stand

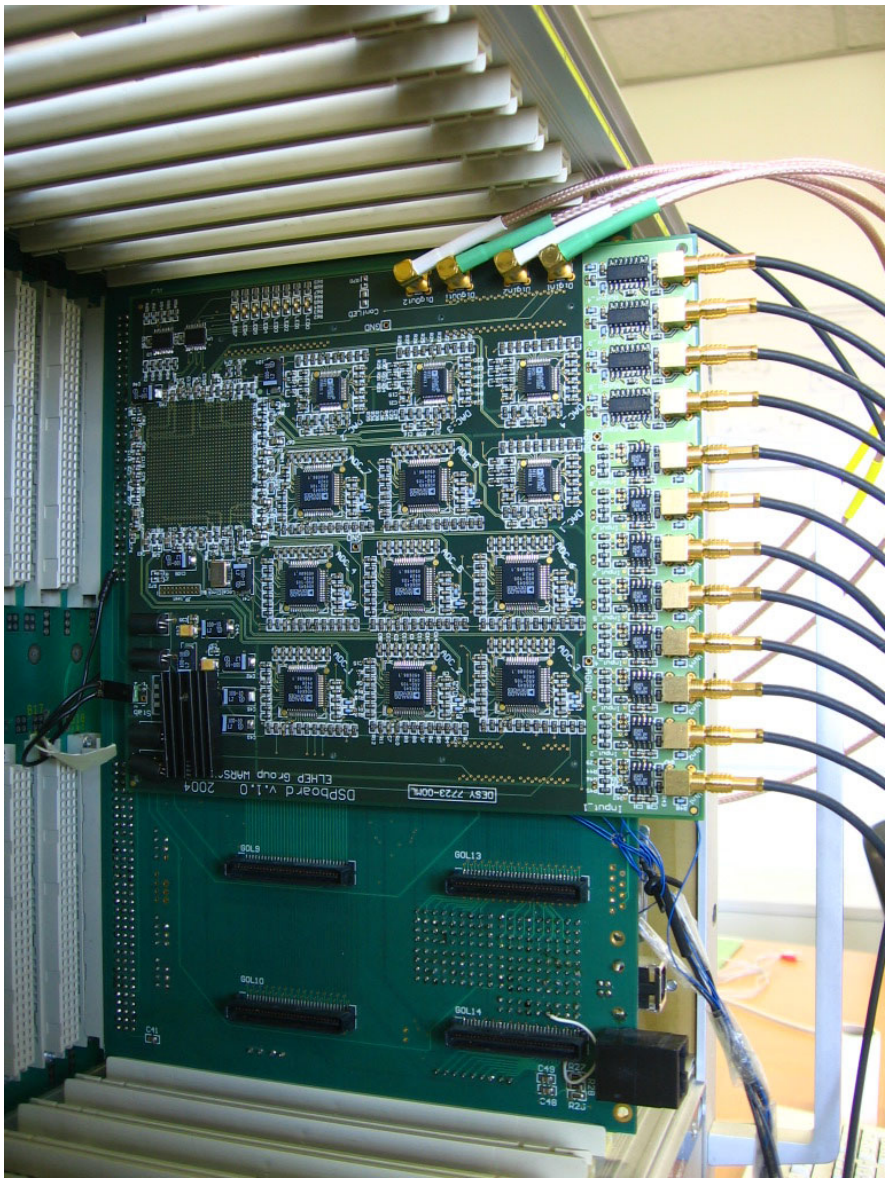

Fig. 19. Full hardware configuration of SIMCON 3.0 and the LLRF-MB platform working in the EURO crate

Fig. 19 presents a full hardware set-up of the SIMCON 3.0 module working together with the LLRF-MB platform. The system is situated in a test and measurement configuration in the EURO crate. The installation was prepared to check the control possibility for the ACC1 module of the VUV FEL SC linac. The SIMCON 3.0 module occupies two upper user's slots in the extension board. The LLRF base-board has still one more slot available.

Now, there are carried out the tests of the LLRF control module at the CHECHIA set-up location and with the ACC1 module. The system is controlled with the software level in the MatLab and DOOCS environments [10]. The readout of measurement signals was performed for all cavities of the ACC1 module. The I and Q signals were detected. The exemplary measurement results were presented in figs. 20 - 22.

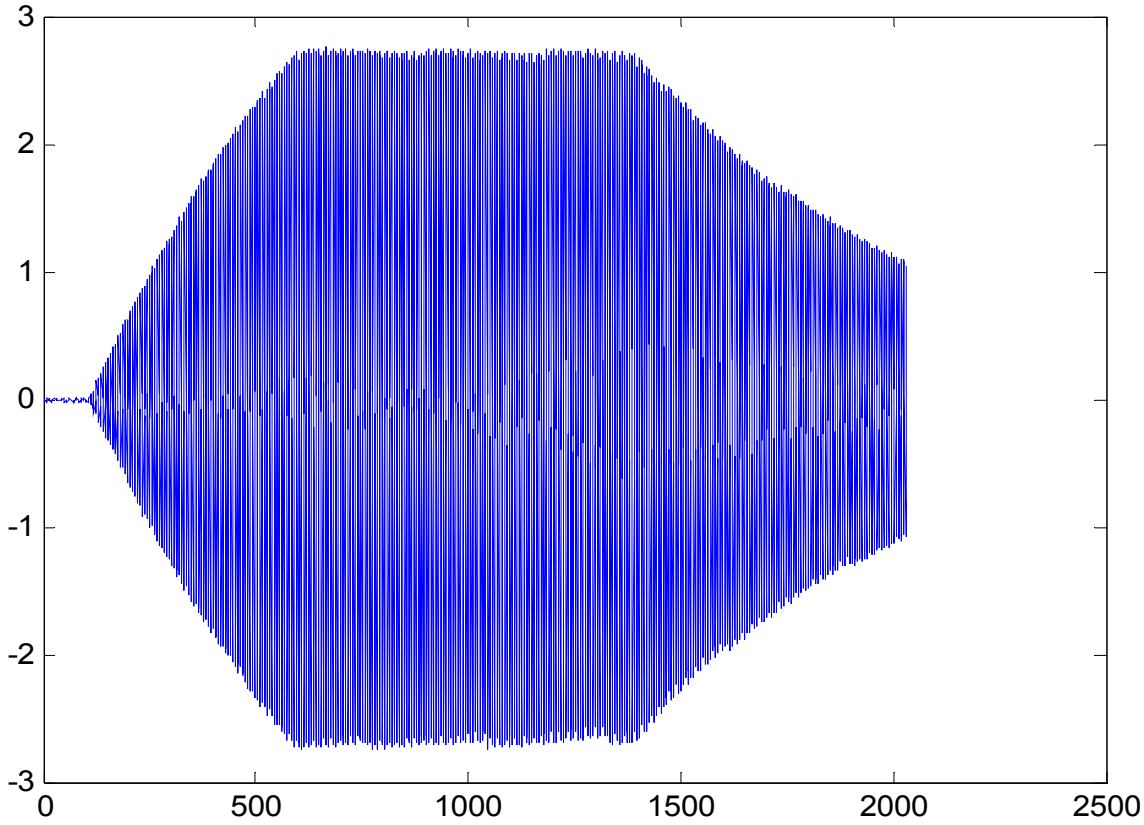

Fig. 20. Readout of the modulated I and Q signal from 1-st cavity of the ACC1 module.

Fig. 20 presents a readout example of the modulated IQ signal from the first cavity of the ACC1 module. The measurement was carried during the time period of 2 ms, with taking samples each 1 μs.

Figures 21 and 22 contain the results of I and Q signals detection by the hardware based DSP algorithm, done in the real-time by the SIMCON 3.0 module.

The positive results of tests and initial investigations of the SIMCON 3.0 parameters and properties enable further research on the next generation of the control system for SC linear accelerators. In particular, it enables a fast replacement of the old DSP processor based system with a fully digital one based on FPGA/DSP chips and fast optical transmission. One of the aims is to be able to change the control method during a single period of the accelerator activity, i.e. in the real-time

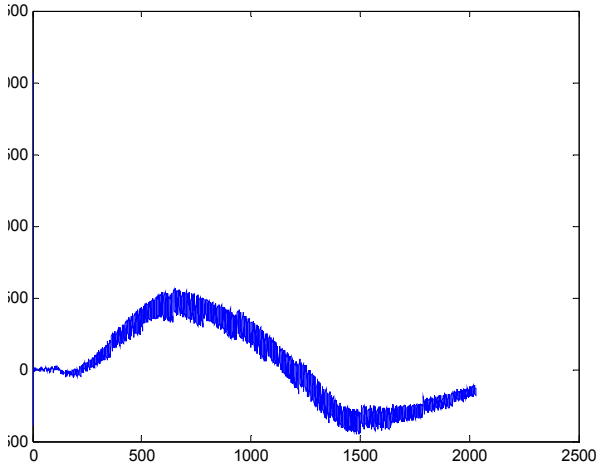

Fig. 21. Detection of I signal from the 1-st cavity of the ACC1 module done by the SIMCON 3.0 system

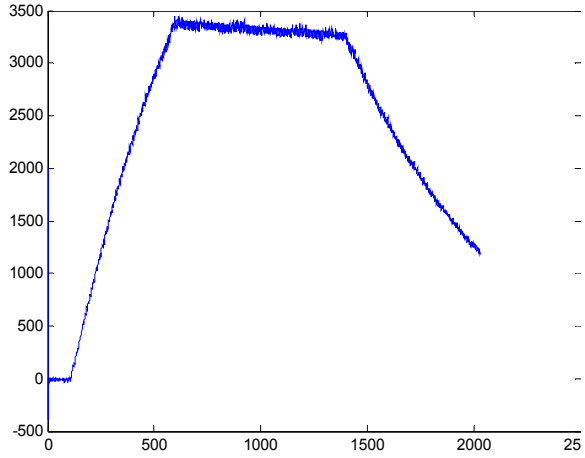

Fig. 22. Detection of Q signal from the 1-st cavity of the ACC1 module done by the SIMCON 3.0 system

6 Technical data of SIMCON 3.0.

The tables, which are presented below, contain the technical data of SIMCON 3.0 system.

6.1 Basic data of SIMCON 3.0.

Table 4 gathers a collection of basic technical data of the SIMCON 3.0 module.

Table 4.
Basic technical data of the eight-channel LLRF control module for SC cavities

Parametr		**Wartość**
Dimensions		162mm x 142mm; thickness 2,3 mm
Analog inputs	Number of channels	8
	Range	± 1V
	Maksimum range of input voltage	± 3.8V
	Range of sampling	Minimum 30 MHz Maximum 105 MHz
	Analog bandwidth	270 MHz
Analog outputs	Number of channels	4
	Range of sampling	Depending on the work mode: from 3 MHz do Makximum 160MHz
	Range of output voltage	± 1V
Digital inputs	Number of	2

	channels	
	level	LVTTL
	Input impedance	50 Ω
Digital outputs	Number of channels	2
	level	LVTTL
Current consumption	Only the board of SIMCON3.0	+5V ≈ 2.04A (+5V ≈ 4A together for DSP-board + Mother-board) +3.3V ≈ 0.32A +1.5V ≈ 0.02A - 12V ≈ 0.4A
Inbuilt clock circuit		60MHz

6.2 A complete list of pins for Xilinx Virtex II 4000 chip

The table contains a description of signals connected to the Xilinx Virtex II 4000 chip. A more precise and full description is in the application data sheets of particular integrated circuits.

Table 5. Signals and pins in Virtex II 4000

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
ADC 1	Data bits	adc_data(1)(0)	U2	
		adc_data(1)(10)	F2	
		adc_data(1)(11)	F3	
		adc_data(1)(12)	G3	
		adc_data(1)(13)	H3	
		adc_data(1)(1)	T2	
		adc_data(1)(2)	P2	
		adc_data(1)(3)	N2	
		adc_data(1)(4)	M2	
		adc_data(1)(5)	L2	
		adc_data(1)(6)	K2	
		adc_data(1)(7)	J2	
		adc_data(1)(8)	H2	
		adc_data(1)(9)	G2	
	differential clock input LVPECL standard (**negative** part)	adc_clk_n(1)	P1	
	differential clock input LVPECL standard (**positive** part)	adc_clk_p(1)	N1	
	Data ready bit	adc_dry(1)	E2	
	Over flow bit	adc_ovr(1)	D2	
ADC 2	Data bits	adc_data(2)(0)	U3	

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
		adc_data(2)(10)	J4	
		adc_data(2)(11)	K4	
		adc_data(2)(12)	L4	
		adc_data(2)(13)	M4	
		adc_data(2)(1)	T3	
		adc_data(2)(2)	R3	
		adc_data(2)(3)	P3	
		adc_data(2)(4)	N3	
		adc_data(2)(5)	M3	
		adc_data(2)(6)	L3	
		adc_data(2)(7)	J3	
		adc_data(2)(8)	F4	
		adc_data(2)(9)	H4	
	differential clock input LVPECL standard (**negative** part)	adc_clk_n(2)	A4	
	differential clock input LVPECL standard (**positive** part)	adc_clk_p(2)	A5	
	Data ready bit	adc_dry(2)	B5	
	Over flow bit	adc_ovr(2)	C8	
ADC 3	Data bits	adc_data(3)(0)	B8	
		adc_data(3)(10)	B16	
		adc_data(3)(11)	A17	
		adc_data(3)(12)	B17	
		adc_data(3)(13)	C16	
		adc_data(3)(1)	B9	
		adc_data(3)(2)	B10	
		adc_data(3)(3)	B11	
		adc_data(3)(4)	B12	
		adc_data(3)(5)	B13	
		adc_data(3)(6)	A13	
		adc_data(3)(7)	B14	
		adc_data(3)(8)	A14	
		adc_data(3)(9)	A15	
	differential clock input LVPECL standard (**negative** part)	adc_clk_n(3)	A11	
	differential clock input LVPECL standard (**positive** part)	adc_clk_p(3)	A12	
	Data ready bit	adc_dry(3)	C14	
	Over flow bit	adc_ovr(3)	D10	
ADC 4	Data bits	adc_data(4)(0)	C6	
		adc_data(4)(10)	D16	
		adc_data(4)(11)	D15	
		adc_data(4)(12)	D14	
		adc_data(4)(13)	D13	
		adc_data(4)(1)	C11	
		adc_data(4)(2)	C12	
		adc_data(4)(3)	C13	
		adc_data(4)(4)	C15	

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
		adc_data(4)(5)	A18	
		adc_data(4)(6)	B18	
		adc_data(4)(7)	C18	
		adc_data(4)(8)	D18	
		adc_data(4)(9)	D17	
	differential clock input LVPECL standard (**negative** part)	adc_clk_n(4)	A21	
	differential clock input LVPECL standard (**positive** part)	adc_clk_p(4)	A22	
	Data ready bit	adc_dry(4)	C27	
	Over flow bit	adc_ovr(4)	D27	
ADC 5	Data bits	adc_data(5)(0)	D19	
		adc_data(5)(10)	C22	
		adc_data(5)(11)	B22	
		adc_data(5)(12)	D23	
		adc_data(5)(13)	C23	
		adc_data(5)(1)	C19	
		adc_data(5)(2)	B19	
		adc_data(5)(3)	D20	
		adc_data(5)(4)	C20	
		adc_data(5)(5)	A20	
		adc_data(5)(6)	D21	
		adc_data(5)(7)	C21	
		adc_data(5)(8)	B21	
		adc_data(5)(9)	D22	
	differential clock input LVPECL standard (**negative** part)	adc_clk_n(5)	A30	
	differential clock input LVPECL standard (**positive** part)	adc_clk_p(5)	A31	
	Data ready bit	adc_dry(5)	C33	
	Over flow bit	adc_ovr(5)	E33	
ADC 6	Data bits	adc_data(6)(0)	B23	
		adc_data(6)(10)	B26	
		adc_data(6)(11)	B27	
		adc_data(6)(12)	B28	
		adc_data(6)(13)	A28	
		adc_data(6)(1)	A23	
		adc_data(6)(2)	D24	
		adc_data(6)(3)	C24	
		adc_data(6)(4)	B24	
		adc_data(6)(5)	A24	
		adc_data(6)(6)	D25	
		adc_data(6)(7)	B25	
		adc_data(6)(8)	D26	
		adc_data(6)(9)	C26	
	differential clock input LVPECL standard (**negative** part)	adc_clk_n(6)	E34	

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
	differential clock input LVPECL standard (**positive** part)	adc_clk_p(6)	D34	
	Data ready bit	adc_dry(6)	C28	
	Over flow bit	adc_ovr(6)	B32	
ADC 7	Data bits	adc_data(7)(0)	A29	
		adc_data(7)(10)	G32	
		adc_data(7)(11)	F33	
		adc_data(7)(12)	H32	
		adc_data(7)(13)	G33	
		adc_data(7)(1)	B29	
		adc_data(7)(2)	C29	
		adc_data(7)(3)	D29	
		adc_data(7)(4)	B30	
		adc_data(7)(5)	B31	
		adc_data(7)(6)	F32	
		adc_data(7)(7)	D32	
		adc_data(7)(8)	D33	
		adc_data(7)(9)	E32	
	differential clock input LVPECL standard (**negative** part)	adc_clk_n(7)	G34	
	differential clock input LVPECL standard (**positive** part)	adc_clk_p(7)	F34	
	Data ready bit	adc_dry(7)	U34	
	Over flow bit	adc_ovr(7)	L32	
ADC 8	Data bits	adc_data(8)(0)	H33	
		adc_data(8)(10)	T33	
		adc_data(8)(11)	U33	
		adc_data(8)(12)	R32	
		adc_data(8)(13)	P32	
		adc_data(8)(1)	J33	
		adc_data(8)(2)	K33	
		adc_data(8)(3)	L33	
		adc_data(8)(4)	M33	
		adc_data(8)(5)	N33	
		adc_data(8)(6)	P33	
		adc_data(8)(7)	N34	
		adc_data(8)(8)	P34	
		adc_data(8)(9)	R34	
	differential clock input LVPECL standard (**negative** part)	adc_clk_n(8)	M34	
	differential clock input LVPECL standard (**positive** part)	adc_clk_p(8)	L34	
	Data ready bit	adc_dry(8)	J34	
	Over flow bit	adc_ovr(8)	N32	
DAC 1	Data bits	dac_data(1)(0)	N31	
		dac_data(1)(10)	W32	
		dac_data(1)(11)	K31	

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
		dac_data(1)(12)	J31	
		dac_data(1)(13)	H31	
		dac_data(1)(1)	M31	
		dac_data(1)(2)	L31	
		dac_data(1)(3)	AB31	
		dac_data(1)(4)	AA31	
		dac_data(1)(5)	Y31	
		dac_data(1)(6)	W31	
		dac_data(1)(7)	V31	
		dac_data(1)(8)	U31	
		dac_data(1)(9)	T31	
	differential clock input LVPECL standard (**negative** part)	dac_clk_n(1)	AC34	
	differential clock input LVPECL standard (**positive** part)	dac_clk_p(1)	AD34	
	DIV0	dac_div(1)(0)	R31	See datasheet for description
	DIV1	dac_div(1)(1)	P31	
	MOD0	dac_mode(1)(0)	V32	
	MOD1	dac_mode(1)(1)	V33	
	PLLLOCK	dac_pll_lock(1)	V34	
DAC 2	Data bits	dac_data(2)(0)	AM4	
		dac_data(2)(10)	AM15	
		dac_data(2)(11)	AP17	
		dac_data(2)(12)	AN17	
		dac_data(2)(13)	AM16	
		dac_data(2)(1)	AL5	
		dac_data(2)(2)	AM6	
		dac_data(2)(3)	AM7	
		dac_data(2)(4)	AM8	
		dac_data(2)(5)	AM9	
		dac_data(2)(6)	AM11	
		dac_data(2)(7)	AM12	
		dac_data(2)(8)	AM13	
		dac_data(2)(9)	AM14	
	differential clock input LVPECL standard (**negative** part)	dac_clk_n(2)	AP31	
	differential clock input LVPECL standard (**positive** part)	dac_clk_p(2)	AP30	
	DIV0	dac_div(2)(0)	AM17	See datasheet for description
	DIV1	dac_div(2)(1)	AL17	
	MOD0	dac_mode(2)(0)	AL6	
	MOD1	dac_mode(2)(1)	AL8	
	PLLLOCK	dac_pll_lock(2)	AL16	
DAC 3	Data bits	dac_data(3)(0)	AA1	
		dac_data(3)(10)	AC3	
		dac_data(3)(11)	AD3	
		dac_data(3)(12)	AF3	
		dac_data(3)(13)	AG3	

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
		dac_data(3)(1)	V2	
		dac_data(3)(2)	W2	
		dac_data(3)(3)	AA2	
		dac_data(3)(4)	AC2	
		dac_data(3)(5)	AH1	
		dac_data(3)(6)	W3	
		dac_data(3)(7)	Y3	
		dac_data(3)(8)	AA3	
		dac_data(3)(9)	AB3	
	differential clock input LVPECL standard (**negative** part)	dac_clk_n(3)	AK34	
	differential clock input LVPECL standard (**positive** part)	dac_clk_p(3)	AL34	
	DIV0	dac_div(3)(0)	AL3	See datasheet for description
	DIV1	dac_div(3)(1)	AK3	
	MOD0	dac_mode(3)(0)	AJ3	
	MOD1	dac_mode(3)(1)	AH3	
	PLLLOCK	dac_pll_lock(3)	AJ4	
DAC 4		dac_data(4)(0)	AL18	
		dac_data(4)(10)	AL27	
		dac_data(4)(11)	AL29	
		dac_data(4)(12)	AL30	
		dac_data(4)(13)	AD31	
	Data bits	dac_data(4)(1)	AL19	
		dac_data(4)(2)	AL20	
		dac_data(4)(3)	AL21	
		dac_data(4)(4)	AL22	
		dac_data(4)(5)	AL23	
		dac_data(4)(6)	AL24	
		dac_data(4)(7)	AN26	
		dac_data(4)(8)	AL25	
		dac_data(4)(9)	AL26	
	differential clock input LVPECL standard (**negative** part)	dac_clk_n(4)	AP24	
	differential clock input LVPECL standard (**positive** part)	dac_clk_p(4)	AP23	
	DIV0	dac_div(4)(0)	AG31	See datasheet for description
	DIV1	dac_div(4)(1)	AF31	
	MOD0	dac_mode(4)(0)	F31	
	MOD1	dac_mode(4)(1)	E31	
	PLLLOCK	dac_pll_lock(4)	AE31	
		ii_addr(0)	AP18	
		ii_addr(10)	AN25	
		ii_addr(11)	AP26	
		ii_addr(12)	AN27	
		ii_addr(13)	AP28	
		ii_addr(14)	AN28	
		ii_addr(15)	AP29	

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
		ii_addr(16)	AN29	
		ii_addr(17)	AN30	
		ii_addr(18)	AN31	
		ii_addr(19)	AN32	
		ii_addr(1)	AN18	
		ii_addr(20)	AM19	
		ii_addr(21)	AM20	
		ii_addr(22)	AM21	
		ii_addr(23)	AM22	
		ii_addr(24)	AM23	
		ii_addr(25)	AM24	
		ii_addr(26)	AM26	
		ii_addr(27)	AM27	
		ii_addr(28)	AM28	
		ii_addr(29)	AM29	
		ii_addr(2)	AN19	
		ii_addr(30)	AM31	
		ii_addr(31)	AM33	
		ii_addr(3)	AP20	
		ii_addr(4)	AN21	
		ii_addr(5)	AP21	
		ii_addr(6)	AP22	
		ii_addr(7)	AN22	
		ii_addr(8)	AN23	
		ii_addr(9)	AN24	
		ii_data(0)	AL32	
		ii_data(10)	AG32	
		ii_data(11)	AG33	
		ii_data(12)	AF32	
		ii_data(13)	AF33	
		ii_data(14)	AF34	
		ii_data(15)	AE33	
		ii_data(16)	AD32	
		ii_data(17)	AD33	
		ii_data(18)	AC32	
		ii_data(19)	AC33	
		ii_data(1)	AL33	
		ii_data(20)	AB32	
		ii_data(21)	AB33	
		ii_data(22)	AB34	
		ii_data(23)	AA32	
		ii_data(24)	AA33	
		ii_data(25)	AA34	
		ii_data(26)	Y32	
		ii_data(27)	Y34	
		ii_data(28)	W33	
		ii_data(29)	AK31	
		ii_data(2)	AK32	
		ii_data(30)	AJ31	
		ii_data(31)	AC31	
		ii_data(3)	AK33	

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
		ii_data(4)	AJ32	
		ii_data(5)	AJ33	
		ii_data(6)	AJ34	
		ii_data(7)	AH32	
		ii_data(8)	AH33	
		ii_data(9)	AH34	
		ii_irqN(0)	M1	
		ii_irqN(1)	L1	
		ii_irqN(2)	J1	
		ii_irqN(3)	G1	
		ii_irqN(4)	F1	
		ii_irqN(5)	C2	
		ii_irqN(6)	B4	
		ii_irqN(7)	A6	
		ii_operN	M32	
		ii_resetN	A26	
		ii_strobeN	E17	
		ii_writeN	D9	
		bus_d(0)	AN16	
		bus_d(10)	AN10	
		bus_d(11)	AN9	
		bus_d(12)	AP9	
		bus_d(13)	AN8	
		bus_d(14)	AN7	
		bus_d(15)	AP7	
		bus_d(16)	AN6	
		bus_d(17)	AP6	
		bus_d(18)	AN5	
		bus_d(19)	AP5	
		bus_d(1)	AP15	
		bus_d(20)	AN4	
		bus_d(21)	AP4	
		bus_d(22)	AN3	
		bus_d(23)	AM2	
		bus_d(24)	AL2	
		bus_d(25)	AL1	
		bus_d(26)	AK2	
		bus_d(27)	AK1	
		bus_d(28)	AJ2	
		bus_d(29)	AJ1	
		bus_d(2)	AN14	
		bus_d(30)	AH2	
		bus_d(31)	AG2	
		bus_d(3)	AP14	
		bus_d(4)	AN13	
		bus_d(5)	AP13	
		bus_d(6)	AN12	
		bus_d(7)	AP12	
		bus_d(8)	AN11	
		bus_d(9)	AP11	
		clk	D12	

part	Signal description	Signal name	Xilinx Virtex II Pin number	remarks
		clkout	D11	
		trgout	B3	
		mclk(0)	B6	
		mclk(1)	T32	
		mclk(2)	J32	
		mclk(3)	B7	
		mtrg(0)	A7	
		mtrg(1)	D8	
		mtrg(2)	D6	
		mtrg(3)	A9	
		ii_ackN	C9	
Local clock		lclk	E19	
Auxiliary LED diodes		led(0)	AB1	
		led(1)	AB2	
		led(2)	AC1	
		led(3)	AD1	
		led(4)	AD2	
		led(5)	AE2	
		led(6)	AF1	
		led(7)	AF2	
		conf_led	AL9	Not mounted
Digital In/out	inputs	sigin(0)	Y1	
		sigin(1)	V1	
	outputs	sigout(0)	U1	
		sigout(1)	R1	
8 bits digital auxiliary port		sigtest(0)	C7	See figure 20.
		sigtest(1)	D3	
		sigtest(2)	E3	
		sigtest(3)	E4	
		sigtest(4)	D1	
		sigtest(5)	E1	
		sigtest(6)	N4	
		sigtest(7)	P4	

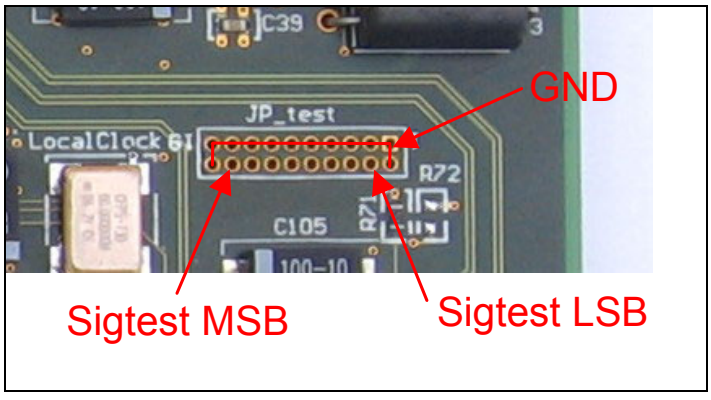

Fig. 23. Digital port signal description

6.3 A list of components for SIMCON 3.0.

Table 6.

Comment	Description	Quantity
AD6644	ADCs	8
100nF	Capacitor	202
0.1uF	Capacitor	8
10nF	Capacitor	24
100pF	Capacitor	4
100uF	Electrolytic Capacitor	9
22uF	Electrolytic Capacitor	4
2.2uF	Capacitor	12
470nF	Capacitor	19
47nF	Capacitor	46
red	LED	1
AD9772A	DACs	4
MCX	BNC Connector	16
FERRITE	coil	4
XC2V4000-4FF1152C	Virtex-II 1.5V Field Programmable Gate Array	1
AMP 32X2	Internal Interface connector	4
-8to-15V (1,2GND)	Header, 2-Pin, Dual row	1
MHDR2X10	Header, 10-Pin, Dual row	1
green	LED	2
yellow	LED	1
LED2	LED	5
65MHz	Local clock	1
GND	spine	3
AGND	spine	2
100	Resistor	224
50	Resistor	24
1k	Resistor	30
3840	Resistor	4
499	Resistor	24
25	Resistor	16
523	Resistor	8
49.9	Resistor	14
0	Resistor	9
187	Resistor	12
LM7905CT	3-Terminal Negative Regulator	1
AD8138	Amplifiler	8
MAX4444	footprint: SO-16	4
74LVT2245	BUS TRANSCEIVER 3SO	2

7 Remarks and recommendations concerning the SIMCON 3.0. PCB design and improvements for SIMCON 3.1.

The design, debugging, testing and commissioning of the SIMCON 3.0 module showed that the analog channels, AD and DA conversions, clock signal distribution, DSP algorithm functions, data acquisition and readout channels, all work properly.

This chapter gathers the major remarks and conclusions concerning the continuous process of developing the current version of the LLRF control system for SC cavity linac. These conclusions are important for the immediately next version of the SIMCON. The following conditions and possibilities were observed:

1. The power losses on the voltage stabilizer and -5V/-12V voltage converter require application of enhanced cooling. The LM7905 voltage stabilizer, positioned on the LLRF-MB was equipped in an additional radiator.
2. Application of intermediate sockets between the LLRF-MB platform and the SIMCON 3.0 module should provide the current flow of 2A. Such a current is needed for 8 ADCs.
3. A few more chassis layers, which is possible technologically, may confine the noise level in the digital part of the system.
4. Application of fast buffers for the differential LVDS and LVPECL lines for additional digital inputs and outputs will increase their pass bands.
5. Positioning of a larger chassis under the DACs and ADCs chips will increase the heat transfer and improve electrical shielding of the EMI generated there
6. Application of the internal control of output impedance in the FPGA Virtex II chips will allow for resignation from the additional external resistors.
7. Temporary blocking of work of the ADCs and DACs will decrease the power losses and will avoid accidental signal values from the outputs of DACs.
8. Application of a precise clock signal distribution system for ADCs and DACs will provide lowering of the jitter to the required level of single picoseconds.
9. Central positioning of the FPGA chip on the PCB will allow for the optimal situation of all the ADCs and DACs. The level of interferences and noises may be minimized by placing the converters near the miniature MCX connectors. The signal can be transmitted to the front panel using the miniature 50 ohm coaxial cables, which will minimise the level of interference for the analog channels.
10. Placing of a separate JTAG socket and a miniature reset button facilitates the work of an operator. A nondependent configuration of FPGA is possible as well as connection of the firmware diagnostic tools.
11. Modern design environments for PCBs enable realization of novel “signal integrity” tests. This test estimates the matching of the paths and transmission lines to a given type of the laminate.

8 Conclusion

The performed tests and measurements of the PCB (of the technical data presented in chapter 6), which were presented in chapter 5 show a considerable technical maturity of the systems. It was shown, in particular, that the SIMCON 3.0 is able to control efficiently, simultaneously a number of superconducting resonant cavities. The total introduced latency of the control loop was measured to be below 1 μs. Lowering the loop latency below the mentioned number allows to introduce a larger amplification in the control loop, even above 100. Now, the maximum value of this parameter, in the control system, basing on the DSP microprocessor, is around 10. It means the increase of one order of magnitude of this value. The quality and bandwidth of the control loop can be increased considerably in the FPGA/DSP/OPTO/PC-EMBEDDED generation of the LLRF system of low latency and high control-loop amplification.

The SIMCON system seems to be ready for long term industrial tests with the working accelerators in different laboratories. These tests should answer a few yet unanswered questions. Some of these questions are:

- How the FPGA based system behaves long-term in the radiation environments?
- Should the new generation digital system base on old VME solutions or try to use less power and less space?
- Should the classical high-quality RF transmission coaxial cables be replaced with fast fiber optic data transmission network connected directly to the FPGA?

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