TESLA Rep-Rate Generator

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This note describes a field programmable gate array used to generate the master timing triggers for the Tesla modulator system. It provides for operating with either 50 or 60 Hz line frequencies.

The TESLA modulator/klystron system is designed to operate at a rep rate of 10 HZ, but sub multiples of the 10 Hz rate will be needed for initial operation of the system. Also TESLA will be operated at Fermilab with the 60 Hz line and at 50 Hz in Europe at DESY. To fill these requirements, TESLA rep rate chassis shown in Figure 1 has been built.

Circuitry in a chassis, shown in Figure 2, first makes a 50/60 Hz pulse train by detecting the positive zero crossings of the ac line. The remaining circuitry is contained in a Field Programmable Gate Array, FPGA. The incoming 50/60 Hz pulse train is divided by five or six to generate a 10 Hz pulse train. The 10 Hz output is used to put an event on a Tevatron-style, TClk, clock generator located in the control system VMEbus crate. Delayed timing signals are then produced by predet timers also in the VMEbus crate.

The modulator requires a *Bouncer* pulse that precedes the *Fire* pulse by about 600 μs. During the modulator output pulse other timing triggers are needed by the rf system and the sample-and-hold chassis. The timing of all of these pulses will be controlled as analog parameters through the control system in the same way as the Linac klystron systems. Delay timing triggers will be generated by predet modules mounted on an IndustryPack™ carrier card in the VMEbus control system crate.

During initial operation of the TESLA system, the repetition rate will be reduced from the nominal 10 Hz. The variable rep rate is selected by a front panel digiswitch as follows:

Switch Position	Output Rep Rate
0	off
1	10 Hz
2	5 Hz
3	2 Hz
4	1 Hz
5	2 Sec
6	5 Sec
7	10 Sec
8	off
9	off

Note that unused switch positions turn off the variable output pulses. During switching transients, the output rep rate should only decrease from the selected rates. Line frequency selection is made by a front panel key switch. The variable rep rate pulses are also placed on the serial TClk signal so that delay timers can be triggered at this rate. The FPGA includes circuitry to insure that successive output pulses cannot be spaced closer than 95 ms. The pinout for the FPGA is shown in Figure 3.

Outputs from the rep rate generator are 1 μs pulses driven by 74F3037 50Ω TTL line drivers. 1ms pulses are internally generated by the FPGA to activate LEDs at both the 10 Hz and the variable rep rate.

Provision for remote control of the rep rate has been added. A four bit rate setting and an eight bit reading are accessed through a rear panel 37-pin "D" connector. The pinout of this connector, shown in Figure 4, matches the digital I/O connector on a rack monitor. The local/remote switch selects the four bits from the digiswitch or the interface connector. At the time each variable output pulse is generated, the count of ten Hz cycles is latched and output on the interface connector. By returning the eight bit reading to the computer, the repetition period is linear. Although three bits are enough to select the allowed rep rate choices, the fourth control bit is included for use as an *inhibit* bit.

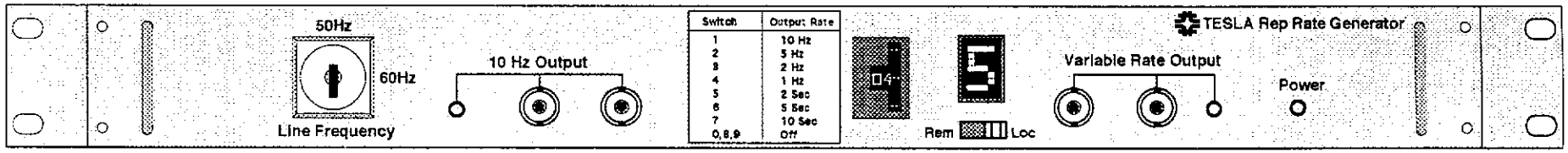
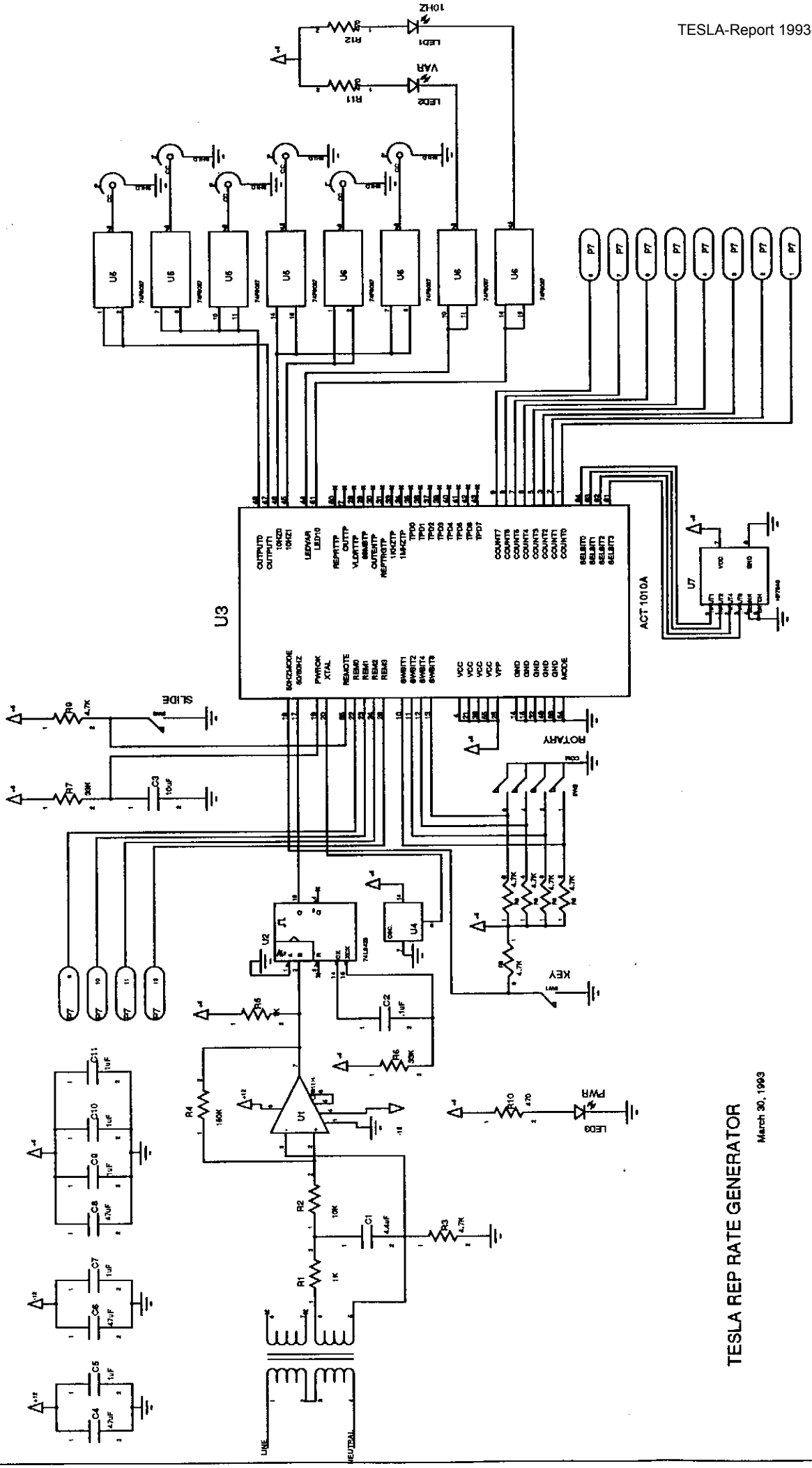


Figure 1. TESLA Rep Rate Generator


TESLA REP RATE GENERATOR
March 30, 1993
U3
ACT1010A
SLIDE
ROTARY
KEY
PWR
LINE
NEUTRAL

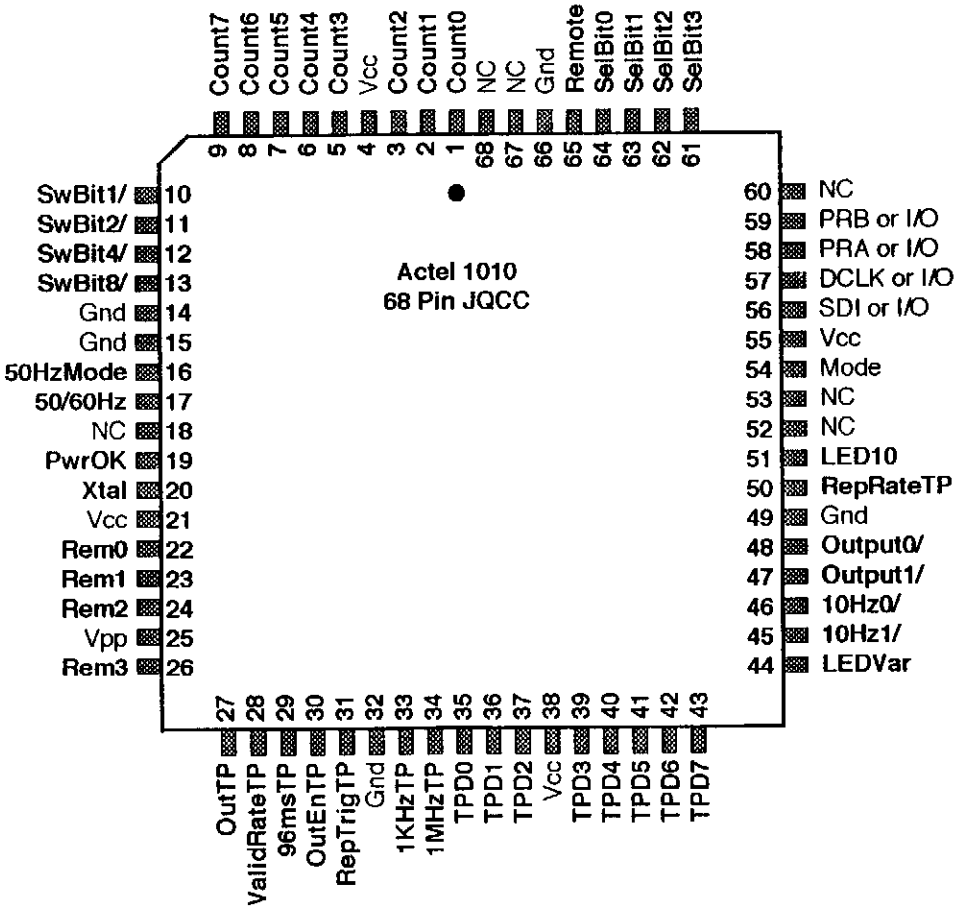


Figure 3. FPGA for TESLA Rep Rate Generator

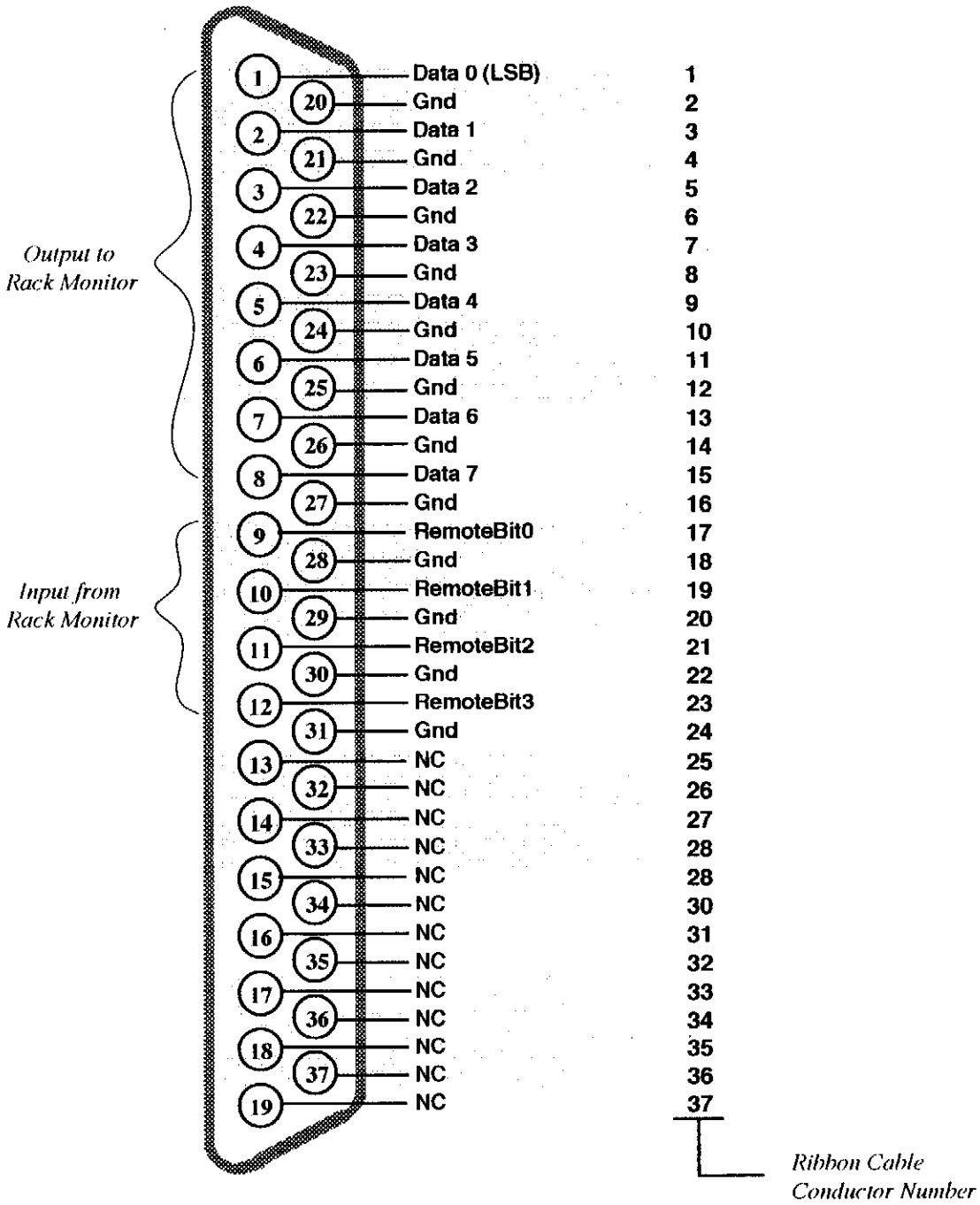


Figure 4. TESLA Rep Rate Generator

Remote Digital Connector Pinout

ms 031293