Stability of the Master Oscillator for FLASH at DESY

Project thesis

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Abstract

In this document a microwave master oscillator (M.O.) and a reference frequency distribution system for the Free Electron Laser (FEL) DESY FLASH is presented. The M.O. generates fixed frequencies ranging from 50 Hz up to 2.856 GHz that must have a defined phase relation. The long term stability (hours) is in the range of a few ps. On short time scales (< 1 sec) the measured timing jitter for generated frequencies higher than 9 MHz is smaller than 100 fs. The focus is on the design of single modules of the M.O.. The established precision measurements techniques used to verify the performance are presented. The measurement results are discussed in the end.

In diesem Dokument wird ein Mikrowellen Master Oszillator (M.O.) für den Freie Elektronen Laser (FEL) DESY FLASH vorgestellt. Im M.O. werden feste Frequenzen zwischen 50 Hz und 2.856 GHz generiert, die eine feste Phasenbeziehung zueinander haben müssen. Die Langzeitstabilität (Stunden) beträgt mehrere ps. Die Kurzzeitstabilität ($<$ 1s) für Frequenzen grösser als 9 MHz ist kleiner als 100 fs. Das Hauptaugenmerk liegt in der Entwicklung der Einzelmodule des M.O. Die Präzisionsmesstechniken um dieses System zu bewerten werden erläutert und die Messergebnisse werden diskutiert.

Contents

1 Motivation

1.1 FLASH and XFEL [1]

In 1993 DESY started developing the next generation linear accelerator using superconducting cavities at an accelerating frequency of 1.3 GHz called Tera Electron-Volts Superconducting Linear Accelerator (TESLA). The accelerated electrons are used for a free electron laser (FEL) to produce coherent X-Ray light of high intensity that has many applications in research for material science, chemistry, biology and other sciences. The XFEL X-ray laser is being planned as a project with European participation. For the project, an all-new research center will be built on the outskirts of the town of Schenefeld (Pinneberg district) in Schleswig-Holstein. Here, the X-ray laser flashes generated in a 3.4-km-long facility will be used for research purposes. The dimensions of the XFEL make it the world's longest artificial light source. A test facility called FLASH is in operation at DESY and gives the opportunity to evaluate technologies for XFEL. With the generation of coherent pulsed X-Ray radiation with wavelengths of a few nanometer and pulswidths smaller than 100 fs it is possible to explore chemical reactions dynamically and the structure of matter at scales of a few nanometers.
Figure 1 sketches the layout of FLASH at DESY.

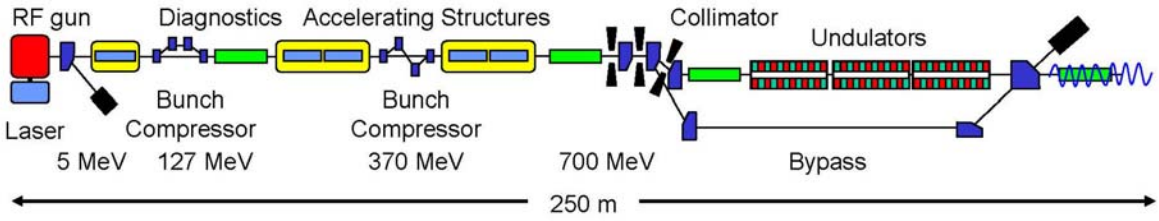

Figure 1:

The generation of coherent X-RAY radiation is based on the SASE - effect (Self Amplified Spontaneous Emission). After an accleration of electron bunches up to several hundreds of MeV the electronbunches enter an undulator where they are forced on a slalom course [2]in which they generate the coherent radiation. The interaction of the induced radiation leads to microbunching inside the electron bunches that are seperated by the wavelength of the radiation. At FLASH a wavelength of 13 nm has been achieved.
The generation of highly coherent radiation is highly sensitive to field and energy fluctuations in the accelerator. Therefore the RF [3] fields in the accelerating structures and the various subsytems have to be synchronized with each other. A Master Oscillator and the distribution system is the source to generate all frequencies synchronous to one reference source in order to obtain the synchronization stability required.

[2]due to the periodicity of north - and south poles of magnets and the resulting Lorenzforce on the electron bunches
[3]Radio Frequency

1.2 Assignment

The various distributed subsystems in the accelerator require a number of different frequencies generated by one source to assure the functionality of the SASE process. The short and long term stability of and between the various widely distributed outputs of the reference system must be in the order of 100 fs and 1 ps respectively [21]. The frequencies are all generated in a reference source that is called the Master Oscillator. The theoretical treatment to judge the stability of this Master Oscillator is studied and has been realized as a prototype for being commisioned at FLASH in late 2006. The single modules are presented here and have been studied in detail.

2 Definition of stability terms

The terms to understand the stability considerations of the reference source mentioned in section 1 are presented here. These are phase noise, integrated timing jitter, drifts and the transport of phase noise through a phase locked loop that serves as a frequency multiplier. For time durations faster than 100 ms one has to investigate the phase noise properties of an RF[4] source and all fluctations slower than 100 ms are denoted as drifts.

2.1 Phase noise description in time and frequency domain

A general description of a carrier frequency ω_0 that is disturbed in amplitude and phase in time domain is:

$$u(t) \;=\; A_0[1 \;+\; \Delta a(t)]\; e^{j\omega_0 t \;+\; j\Delta\varphi(t)} \tag{1}$$

where $\Delta a(t)$ is the instantaneous contribution of amplitude fluctuations and $\Delta\varphi(t)$ is the contribution of phase fluctuations. The further description assumes much smaller amplitude fluctuations than phase fluctuations ($\Delta a(t) \;<<\; 1$) so the above equation reduces to:

$$u(t) \;=\; A_0\; e^{j\omega_0 t \;+\; j\Delta\varphi(t)} \tag{2}$$

The description of the phase fluctuations at carrier frequency ω_0 in frequency domain is the fourier transform of equation 2 where $u(t)$ has been replaced by $\varphi(t)$ to describe only the phae fluctuations and reads:

$$S_\varphi \;=\; \lim_{T\to\infty} \frac{1}{T} |\mathfrak{F}_t\{\varphi(t)\}|^2 \tag{3}$$

This is called the phase power spectral density and can be calculated analogous to the voltage power spectral density [8] where $\mathfrak{F}_t\{\varphi(t)\}$ denotes the fourier transform of $\varphi(t)$ and reads:

$$\mathfrak{F}_t\{\varphi(t)\} = \int_{-T}^{T} \varphi(t) e^{-j\omega t} dt \tag{4}$$

In order to determine the phase power spectral density 3 one has to measure the single sideband phasenoise $\mathscr{L}_\varphi(f)$ of the source. The phase power spectral density and the single sideband phase noise differ by a factor of two in the case $\Delta\varphi(t) \;<<\; 1$:

$$S_\varphi(f) \;=\; 2\mathscr{L}_\varphi(f) \tag{5}$$

It describes the short term fluctuations of RF and microwave oscillators at carrier frequencies ranging from 10 MHz to several GHz. An ideal frequency source is just a delta function at ω_0 in frequency domain but the real source shows fluctuations that lead to the so called "noise skirts" around the main carrier [4] The noise skirts far away from the carrier $f_{offset} \;>\; 5\; MHz$ shows the noise floor that is called white noise or johnson noise. Closer to the carrier the noise increases and follows a $1/f$ and again coming closer a $1/f^2$ and a $1/f^3$ law. Phase Noise is measured in $\frac{dB_c}{Hz}$ which accounts for the noise power related to the carrier measured at a given offsetfrequency in a normalized bandwidth of 1 Hz.

A useful method for modeling the "noise skirts" is to describe them as small phase modulation at offset frequencies from the carrier in a bandwidth of 1 Hz. The interested reader may refer to [4], [19] or [20].

[4] Radio Frequency

2.2 Transmission of amplitude - and phase noise in linear networks

To describe the transmission of amplitude - and phase noise from the input to the output in a linear network one makes use of a conversion matrix equation 6 that relates the amplitude - and phase fluctuations at the input of the network to the output of the network.

$$\underbrace{\begin{bmatrix} \frac{\Delta a_{out}}{A_0} \\ \Delta\varphi_{out} \end{bmatrix}}_{noisy\ output} = \underbrace{\begin{bmatrix} K_{aa} & K_{a\varphi} \\ K_{\varphi a} & K_{\varphi\varphi} \end{bmatrix}}_{conversion\ matrix} \underbrace{\begin{bmatrix} \frac{\Delta a_{in}}{A_0} \\ \Delta\varphi_{in} \end{bmatrix}}_{noisy\ input} + \underbrace{\begin{bmatrix} \frac{\Delta a_{network}}{A_0} \\ \Delta\varphi_{network} \end{bmatrix}}_{noisy\ network} \tag{6}$$

Amplitude - and phase fluctuations are phasors describing the noise as an AM[5] Δa and PM[6] $\Delta\varphi$ at an offsetfrequency $\Delta\omega$ from the carrier ω_0 [5]. The amplitude of the AM contribution is normalized to the carrier voltage A_0.

The input amplitude - and phase noise is directly converted by the factors K_{aa} and $K_{\varphi\varphi}$. The factors $K_{a\varphi}$ and $K_{\varphi a}$ describe how an AM converts to a PM and how a PM converts to an AM. The additional vector accounts for the AM and PM noise contribution of the network.

2.3 Phase noise in a mutiplier chain

An input phase noise $\Delta\varphi_{in}(t)$ is converted by an ideal multiplier N to the output $\Delta\varphi_{out}(t)$ that means that $K_{\varphi\varphi} = N$. Assuming that $K_{a\varphi} = 0$ and the multiplier is ideal the equation describing this reads:

$$\Delta\varphi_{out}(t) = N\ \Delta\varphi_{in}(t) \tag{7}$$

The spectral densities are gained from equation 3 and read:

$$S_{\varphi_{out}}(f) = N^2\ S_{\varphi_{in}}(f) \tag{8}$$

The assumption of an ideal multiplier is not valid in all circumstances since the network will add it's own noise to the output e.g. especially 1/f noise is a big noise source in semiconductors.

2.4 Phase noise model of a phase locked loop

A common method to generate high stable reference frequencies is to make use of a phase locked loop (PLL). This will reduce the overall output power spectral density as derived in the previous section. The output frequency is phase locked to a reference source at a lower frequency [2.4]. The modeling of phase noise in a PLL follows the description in [2]. This model describes how the phase noise of the reference ($S_{\varphi\ REF}(f)$) and the VCO ($S_{\varphi\ VCO}(f)$) are filtered by the loop transfer function. This model excludes noise sources in the Phasedetector (PD), Loop Filter (LF) and Frequency divider (N).

[5] Amplitude Modulation
[6] Phase Modulation

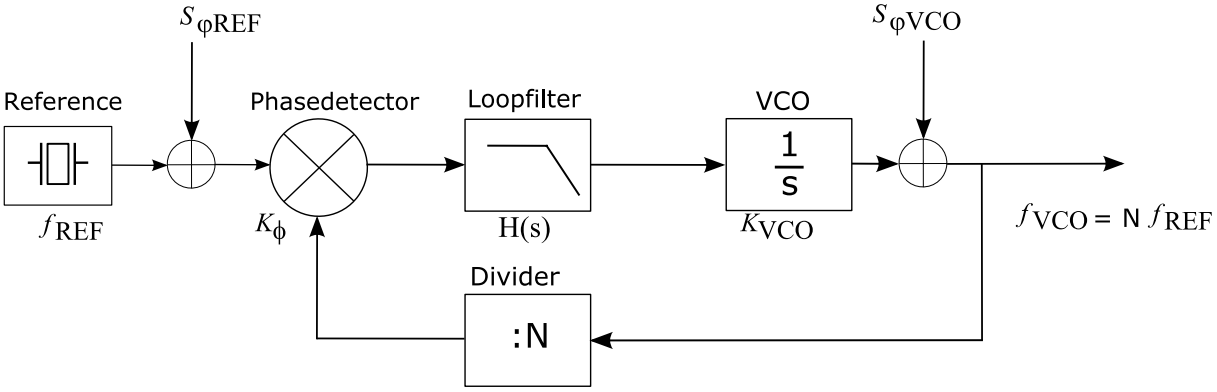

Figure 2: Phase noise model of the PLL

It follows the derivation of the phase transfer function of the PLL.
At point A in figure 2.4 the phase fluctuations from the VCO are scaled down with N to obtain a phase/frequency comparable with the reference input phase Φ_{REF} at the input of the phase detector:

$$\Phi_A(s) \;=\; \frac{\Phi_{VCO}(s)}{N} \tag{9}$$

The output of the phasedetector (point B) delivers an error voltage $V_B(s)$ proportional to the phase difference between $\frac{\Phi_{VCO}(s)}{N}$ and $\Phi_{REF}(s)$ where the proportinality factor is the phasedetector constant K_Φ:

$$V_B(s) \;=\; K_\Phi(\Phi_{REF}(s) \;-\; \frac{\Phi_{VCO}(s)}{N}) \tag{10}$$

The error voltage is filtered by the filter transfer function $H(s)$ and applied to the VCO

$$V_C(s) \;=\; H(s)K_\Phi\left[\Phi_R(s) \;-\; \frac{\Phi_{VCO}(s)}{N}\right] \tag{11}$$

For the overall transfer function the VCO adds its internal noise source:

$$\Phi_{VCO}(s) \;=\; K_{VCO}V_C(s) \;=\; \frac{K_{VCO}H(s)K_\Phi}{s}\left[\Phi_R(s) \;-\; \frac{\Phi_{VCO}(s)}{N}\right] \;+\; \Phi_0(s) \tag{12}$$

With the abbreviation

$$K \;=\; \frac{K_{VCO}K_\Phi}{N} \tag{13}$$

the equation 12 simplifies to

$$\Phi_{PLL}(s) \;=\; \left[\frac{s}{s \;+\; KH(s)}\right]\Phi_{VCO}(s) \;+\; \left[\frac{NKH(s)}{s \;+\; KH(s)}\right]\Phi_{REF}(s). \tag{14}$$

Or expressed in terms of power spectral densities one has to square the transfer function properties of the phase locked loop:

$$S_{\varphi_{PLL}}(f) = |H_0(f)|^2 S_{\varphi_{VCO}}(f) + N^2|H_{REF}(f)|^2 S_{\varphi_{REF}}(f) \tag{15}$$

The equation states that the reference power spectral density $S_{\varphi_{Ref}}$ is low-pass filtered and the VCO power spectral density $S_{\varphi_{VCO}}$ is high-pass filtered which means that both densities contribute to the overall phase noise characteristics of the PLL. It is now the job of the developer to find the most appropriate loop filter $H(s)$ for the application.

2.5 Integrated phase noise and timing jitter

An important figure of stability is not only the definite phase noise at offsetfrequencies of an RF source but also the integrated phase noise and the integrated timing jitter. For a measured phasenoise characteristic $\mathscr{L}_\varphi(f)$ the integrated phase noise can be calculated as follows:

$$\Delta\phi = \sqrt{\int_{f_1}^{f_2} S_\varphi(f)df}\ [rad]_{rms} \tag{16}$$

where $S_\varphi(f)$ is two times the single sideband phase noise $\mathscr{L}_\varphi(f)$ and f_1 and f_2 denote the bandwidth over which the noise has to be integrated. The integrated phase noise (equation 16) can be related to the carrier f_0 under consideration and give the integrated timing jitter:

$$\Delta T_{rms} \ = \ \frac{1}{2\pi f_0}\sqrt{\int_{f_1}^{f_2} S_\varphi(f)df}\ [s]_{rms} \tag{17}$$

A lower integration limit f_1 of 10 Hz corresponds to an error in an observation time faster than 100 ms. If one wishes to investigate the stability of a source within 1 second one has to integrate from 1 Hz up to the upper frequency limit given by f_2. For the stability considerations discussed for the Master Oscillator in section 4 the lower limit f_1 is at 10 Hz and the upper limit f_2 is at 1 MHz.

2.6 Drifts

Drifts is the long term stability of an RF source and their related phases at distances ranging from a few meters up to hundreds of meter inside the accelerator facility. It is a measure to determine how different frequencies generated in one source change their phase relation. This change of the phase is mainly caused by the change of temperature. The quantification of these drifts is given as a temporal variation of a carrier phase caused by temperature changes:

$$drifts\left[\frac{sec}{^\circ C}\right] \ = \ \frac{\Delta t}{\Delta T}\left[\frac{s}{^\circ C}\right] \tag{18}$$

A temperature change of 10 $^\circ C$ leads to an increasing change of phase expressed in portions of the carrier period.

3 Measurement principles

The measurement principles to evaluate the system under consideration are discussed in this chapter. For phase noise there have been many "old fashioned" approaches like the delay line method [14], the direct method with spectrum analyzer [15] where in both methods you only need one source to characterize the phase noise and the PLL method [20] in which you need two sources to characterize the phase noise of your source. All methods have advantages and disadvantages and are summarized in detail in [4]. The measurement principle used here is a cross correlation method realized in the measurement device called E5052 by Agilent Technologies. The studies of the drifts is a topic dealing with the temperature dependent behavior of devices in the Master Oscillator and the distribution system and causes big problems for the stabilization of phases in the accelerator. Several drift measurement methods to verify the performance of subcomponents and the complete system are presented here.

3.1 Phase Noise measurement using cross correlation

The measurement method implemented in the E5052 is comprised of two independent downconverter chains with local oscillators LO_1 and LO_2. The setup is sketched in figure 3.1.

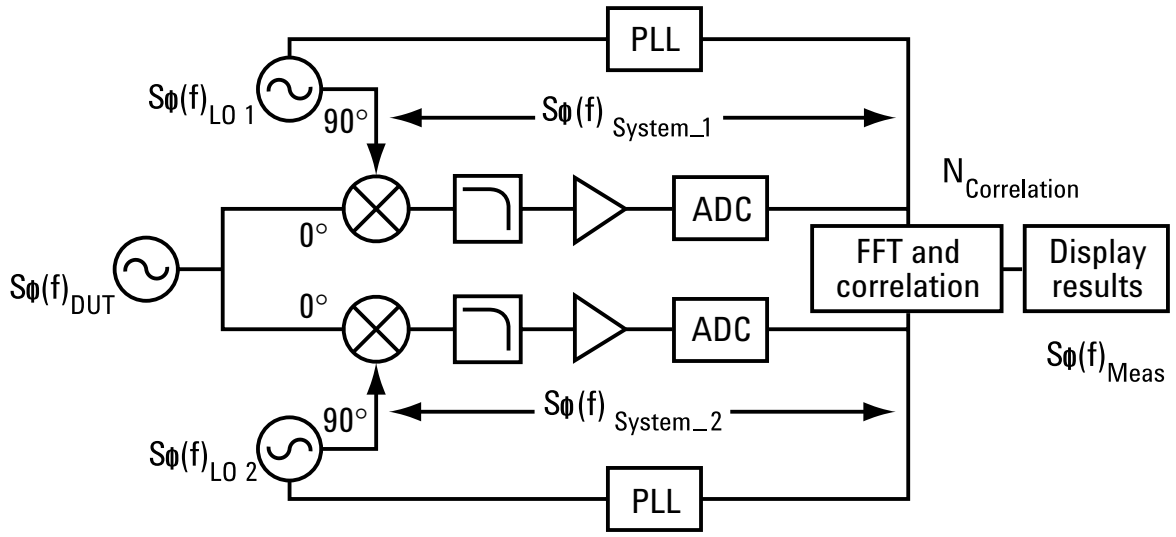

Figure 3: Measurement principle using cross correlation (picture:[18])

The total measured phase noise floor of this device can be reduced by the factor of $\sqrt{N}$ according equation 19. The factor N is the number of measurements that have been made to reduce the noise floor of the device.

$$S_\varphi(f)_{Meas} = S_\varphi(f)_{DUT} + \frac{S_\varphi(f)_{LO_1} + S_\varphi(f)_{LO_2} + S_\varphi(f)_{System_1} + S_\varphi(f)_{System_2}}{\sqrt{N_{Correlation}}}[19] \quad (19)$$

3.2 Drift measurement methods

3.2.1 Principle operation of a phasedetector

The principle measurement method to characterize drift contribution of RF sources and the electronics behind it is based on measuring the phase variation of two RF sources. Figure 4 illustrates the phasedetector that is symbolized by a common mixer symbol.

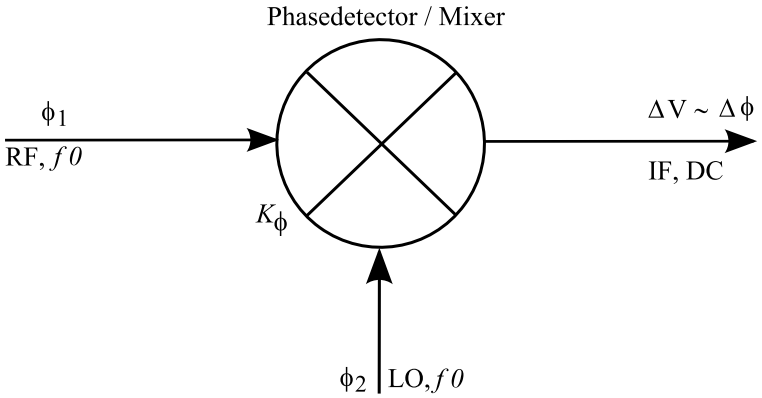

Figure 4: Phasedetector and mixer

In the case of using a double balanced mixer the inputs of the detector are the local oscillator LO and the radio frequency RF input. In the drift measurement setup 3.2.2 the two inputs have the same frequency f_0. The output voltage of the phasedetector is proportional to the phasedifference $\Delta\phi$ of the two input phases ϕ_1 of the RF and ϕ_2 of the LO. The proportionality factor is called the phasedetector gain K_ϕ and is given in $\frac{V}{rad}$ or respectively $\frac{V}{^\circ}$.

The output voltage versus phasedifference of a typical phasedetector is shown in figure 5.

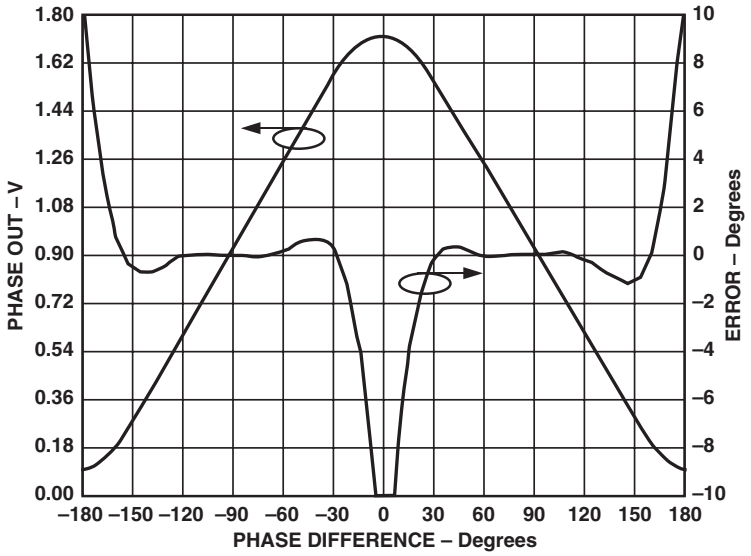

Figure 5: Slope of AD8302 and phase error [6]

For this detector the K_ϕ can be found as $\frac{1.8\ V}{180\ ^\circ} = \frac{10\ mV}{^\circ}$. From this plot it can also be seen that for phase differences leading to voltages at the lower corner of 0 V or the upper end of the detector 1.8 V the phase error of the detector is significantly increased. To minimize

nonlinear distortions the operating point should be chosen such that the detector works at an operating point from 500 mV up to 1.4 V. The operating point can be adjusted by introducing a phase shift of the RF input phase ϕ_1 and ϕ_2 by adjusting the cable length or by using a phase shifter. A factor of $\frac{\lambda_{eff}}{4}$ [7] as the length difference between the two cables will not only lead to the smallest phase errors but also gives the maximum sensitivity to detect phase variations [4].

3.2.2 Drifts of a phase detector

The phase detector AD8302 from Analog Devices is found to have the smallest drift contribution from commercially available phasedetectors. A measurement setup to find out the drifts of a phasedetector is sketched in figure 6.

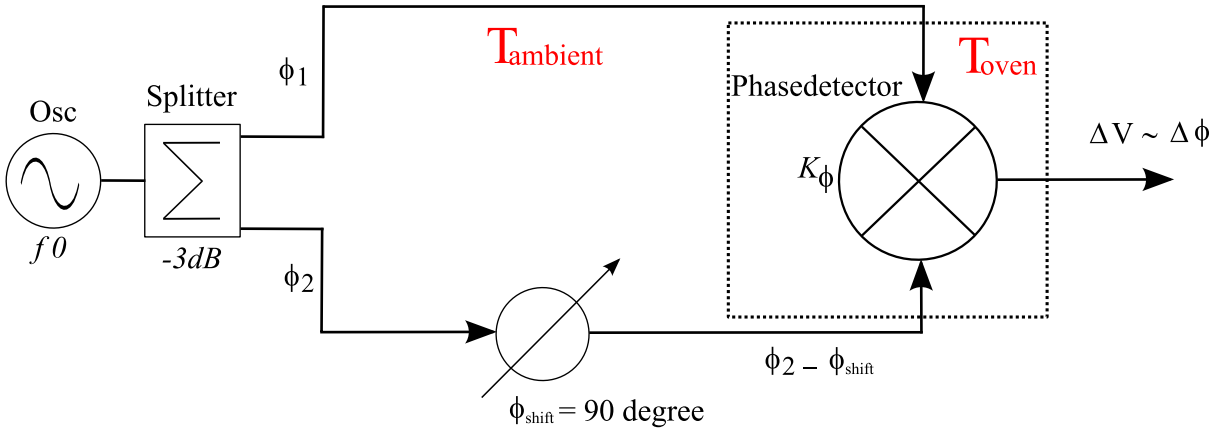

Figure 6: Phase measurement setup

An RF source with f_0 and the period $T_0 = \frac{1}{f_0}$ is split into two branches with the corresponding phases ϕ_1 and ϕ_2. The phase ϕ_2 gets an additional phase shift of 90° to minimize the phaserrors of the phasedetector. The phasedetector converts the phasedifference $\Delta\phi = \phi_1 - \phi_2 - 90°$ with a conversion gain of K_ϕ to a proportional voltage ΔV.

$$\Delta V = K_\phi \, \Delta\phi \tag{20}$$

The phasedetector is put into an oven at temperature T_{Oven} with a temperature profile sketched in figure 7. The other equipment of the setup is held at constant ambient temperature $T_{ambient}$.

[7] where λ_{eff} denotes the effective wavelength of the RF input frequency in the coaxial cable

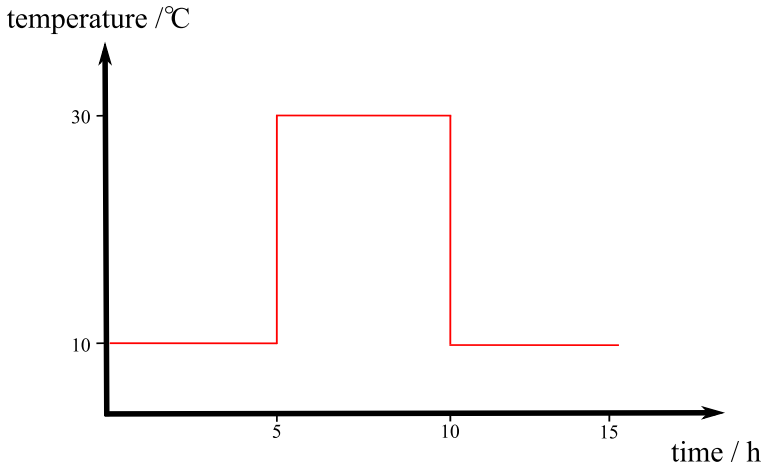

Figure 7: Temperature profile T_{Oven}

The temperature step invoked voltage fluctuations ΔV and therefore the $\Delta\phi = \phi_1 - \phi_2 - 90°$ is only depending on the fluctuations added by the phasedetector itself based on the assumption that the splitter, the cables and the phaseshifter do not contribute to the phase fluctuations. This can be illustrated by the model illustrated in figure [8] that assumes a linear conversion of the related input phases.

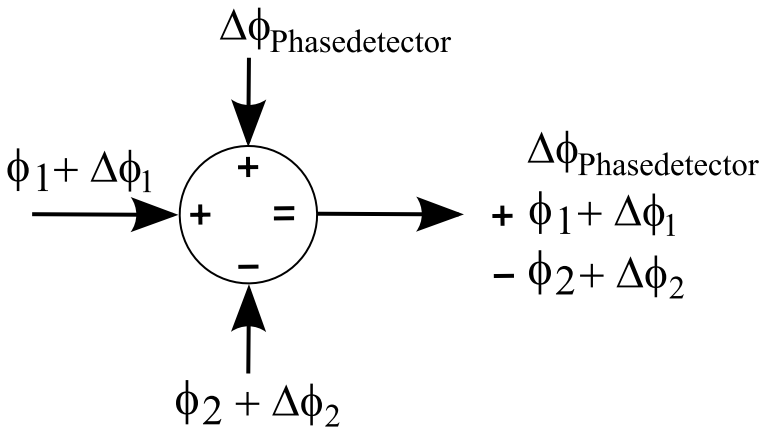

Figure 8: Phase error budget

The phases ϕ_1 and ϕ_2 will subtract from each other and lead to a constant phase offset depending on the phaseshift of the phase shifter that is adjusted in a manner mentioned above 3.2.1. The amount of the related phase fluctuations $\Delta\phi_1$ and $\Delta\phi_2$ originate from the same source and therefore will subtract as well from each other and will not contribute to a phase fluctuation at the output. The remaining fluctuations originate in the phasedetector $\Delta\phi_{Phasedetector}$.
The measurements are converted to $\Delta\phi_{Phasedetector}$ with formula 20 and then read

$$\Delta\phi_{Phasedetector} = \frac{\Delta V}{K_\phi}. \tag{21}$$

These are again converted to the fluctuations of the RF carrier ΔT as a portion of the RF carrier period T_0:

$$\Delta T = \frac{\Delta\phi}{360°} T_0 \tag{22}$$

For a temperature step of 20 $°C$ as sketched in figure [7] the output shows fluctuations in $\frac{\Delta V}{20°C}$. With this procedure the inertial stability of the phasedetector is found out. For maximizing the stability of the phase detector it has to be temperature stabilized. From the stability requirement of the entire Master Oscillator system in section 4.1 the accuracy requirement for the phasedetector can be estimated. As a rule of thumb it has to be at least 10 times better than what is required for the whole Master Oscillator system.
Evaluation measurements show [12] that a drift stability of less than 50 fs at a constant temperature of the phasedetector can be achieved with the AD8302.

3.2.3 Drifts of an amplifier

The drift properties of an ampifier can be characterized by using a phasedetector described in the previous section 3.2.2. The measurement setup for measuring amplifier drifts is sketched in figure 9.

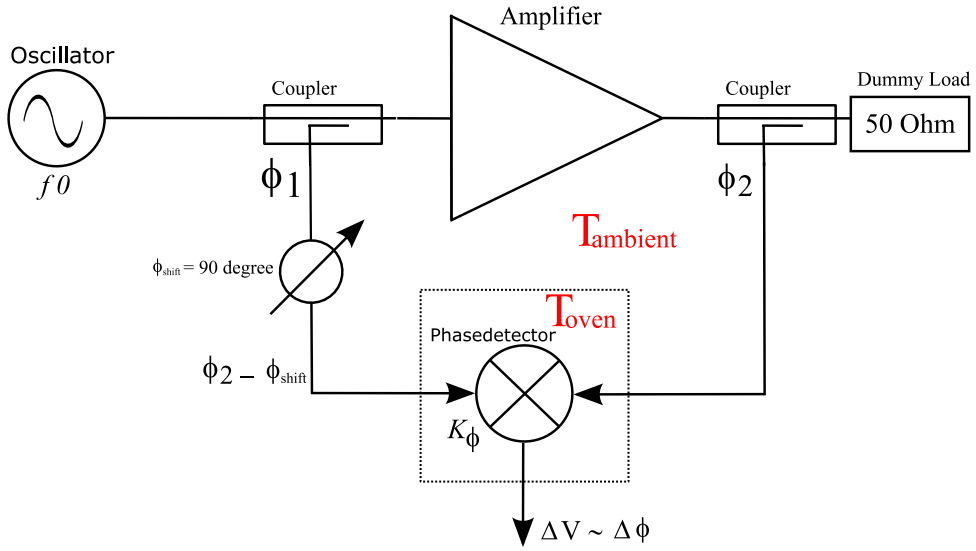

Figure 9: Drift measurement setup of an amplifier

The measurement procedure equals the description for measuring the internal phase drifts of a phasedetector. When stabilizing the phasedetector at a fixed temperature 25 $°C$ the fluctuations of the phasedetector are neglectible compared to the drifts of the amplifier.

3.2.4 Drifts of several RF sources

A source generating several frequencies at the same time can also be characterized concerning its drifts. The measurement setup is sketched in figure 10. A reference oscillator is a reference for two equal oscillator systems generating the outputfrequencies $f_0,\ f_1,\ f_2,\ \ldots,\ f_n$. The output phases are compared with phasedetectors $PD_0,\ PD_1,\ PD_2,\ \ldots, PD_n$ that are stabilized in temperature at T_{Oven} so drift contributions from the Phasedetector are neglectible in the range of what has been shown in section 3.2.2. Assuming that the input phases $\phi_{input\ 1}$ and $\phi_{input\ 2}$ for the two oscillators remain constant for a neglectible environmental temperature change a temperature step on oscillator 1 with a temperature profile $T_{chamber}$ as used to characterize the phasedetector will give us the temperature dependence of the drifts at frequencies $f_0,\ f_1,\ f_2,\ \ldots,\ f_n$.

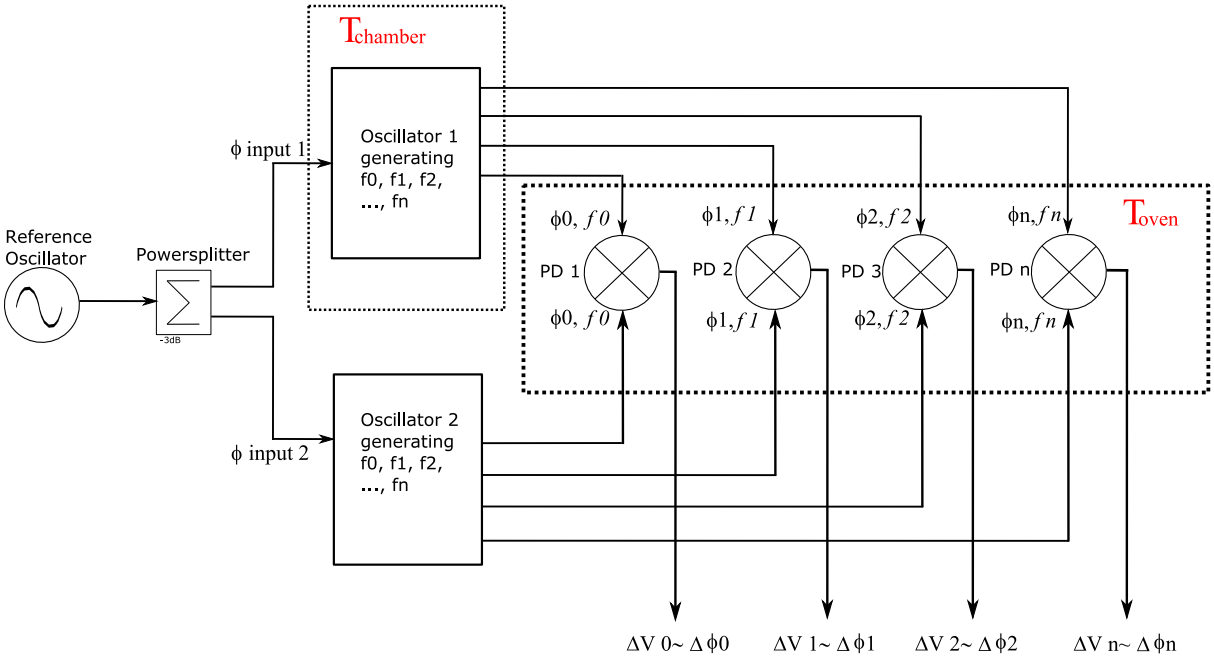

Figure 10: Measurement setup to estimate drifts of two oscillator systems against each other

This setup will be used to judge the performance of the oscillator system as a whole but will not localize the limiting electronic components inside the box.

4 Master Oscillator

The challenging task of generating all frequencies needed in the accelerator facility with a short term stability of $\Delta T = 100\ fs$ and a long term stability in the range of a few picoseconds is in the focus of this chapter. First an overview of the M.O. and the distribution system is given including a table of frequencies with required output powers. The socalled Low Power part (LPP), 1.3 GHz PLL, 2.856 GHz PLL, High Power Part 1.3 GHz (HPP), High Power Part 81 MHz (HPP) are presented here.
The phase noise performance and the related minimization of the integrated timing jitter with the help of phase locked loops is focused on. An important issue of the PLL is its stability that also has been studied. A comparison of required and achieved parameters is put in the summary of the thesis.

4.1 Overview

The overview of the entire system is sketched in figure 4.1 and is composed of the Master Oscillator where all frequencies are generated and the distribution system that links the M.O. with subsystems in the facility and an optical phase drift monitoring system developed by [11].

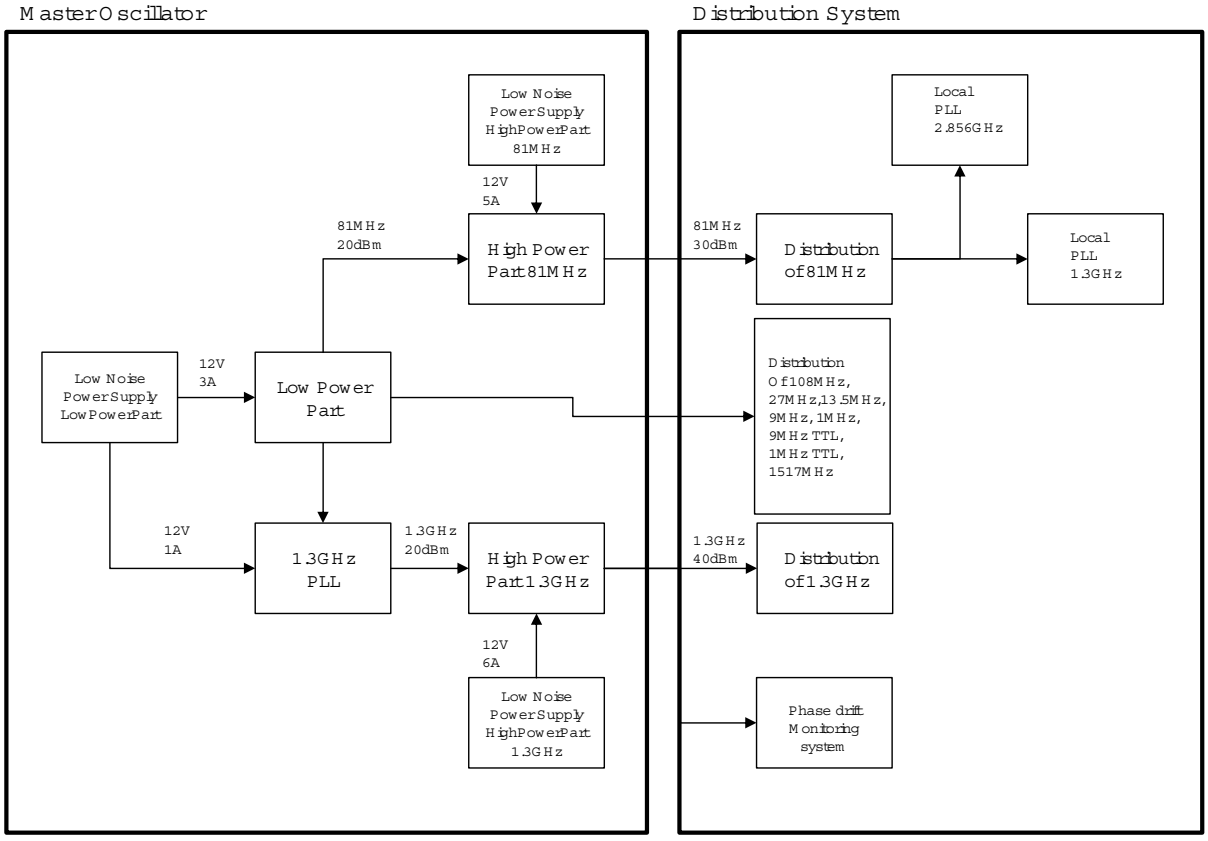

Figure 11: Master Oscillator and distribution system

The frequencies required in the FLASH facility at DESY are listed in table 1:

Output frequencies [MHz]	Power levels [dBm]	Powers required
81.249975 (1)	19.23	20
81.249975 (2)	19.47	20
81.249975 (3)	19.6	20
81.249975 (4) [8]	17.66	20
81.249975 Monitor	0.324	0
108.3333 (1)	18.55	20
108.3333 (2)	18.6	20
108.3333 (3)	18.85	20
108.3333 (4) [9]	16.58	20
108.3333 Monitor	-1.55	0
1	4.87	8
9.027775 (1)	21.93	20
9.027775 (2)	22.02	20
9.027775 (3)	22.03	20
9.027775 (4)	22.02	20
13.5416625 (1)	10.03	8
13.5416625 (2)	9.96	8
27.083325 (1)	12.27	11
27.083325 (2)	12.18	11
1299.9996	19	20
2856.001105	15	20
81.249975 [10]	30	30
1299.9996 [11]	40	40

Table 1: Output powers from Master Oscillator

The requirements for the system including the distribution [12] are for the short term 100 fs and for the long term 1 ps respectively [21]. The short term is defined for an integration bandwidth from 10 Hz...1 MHz and is specified in terms of phase noise for three different frequencies also found in the specification [21]. A comparison of phase noise characteristics will be made when discussing the single modules in the M.O. in the following.

[8] goes through two couplers
[9] goes through two couplers
[10] after amplification by HPP 81 MHz
[11] after amplification by HPP 1300 MHz
[12] not considered here

4.2 Low Power Part

The system frequency of FLASH is the resonance frequency of the resonant cavities to accelerate the electrons which exactly is

$$1.3\ GHz - 400\ Hz = 1.2999996\ GHz^{13}. \tag{23}$$

To generate a source with an integrated timing jitter of less than 100 fs [14] one has to find a proper design that leads to the required phase noise characteristics or respectively timing jitter. The design considerations are discussed in the following chapters. To achieve the required performance a cascade of phase locked loops has been chosen which results in a high long term stability and high small term stability.
The main source of the M.O. is an OCXO operating at 9.0277775 MHz which is multiplied by a cascade of two PLL's with a factor of N = 144 to obtain the main resonance frequency of 1.2999996 GHz. A detailed overview of the M.O. low power part is sketched in figure 12. The modules of the Low Power Part (LLP) of the Master Oscillator are the reference OCXO at 9.027775 MHz, the two PLL's for stabilizing the 81 MHz and 108 MHz VCXO's, the divider modules to divide 81 MHz by a factor of 9 to generate 9 MHz and divide 81 MHz by a factor of 3 to generate 27 MHz. The 81 / 9 divider modules deliver a 9 MHz ECL reference signal for the divider module 9 / 1 that generates a 1 MHz signal. The 81 / 3 divider modules deliver a 27 MHz reference signal for the divider module 27 / 2 that generates a 13.5 MHz signal. The output signals of the 81 / 9 and 9 / 1 divider modules are used as reference signals for the 9 MHz and 1 MHz TTL drivers. One output of the 108 MHz VCXO is a reference signal for generating 50 Hz with a DDS module.

[13] 400 Hz is the bandwidth of the cavities
[14] Δf = 10 Hz...1 MHz

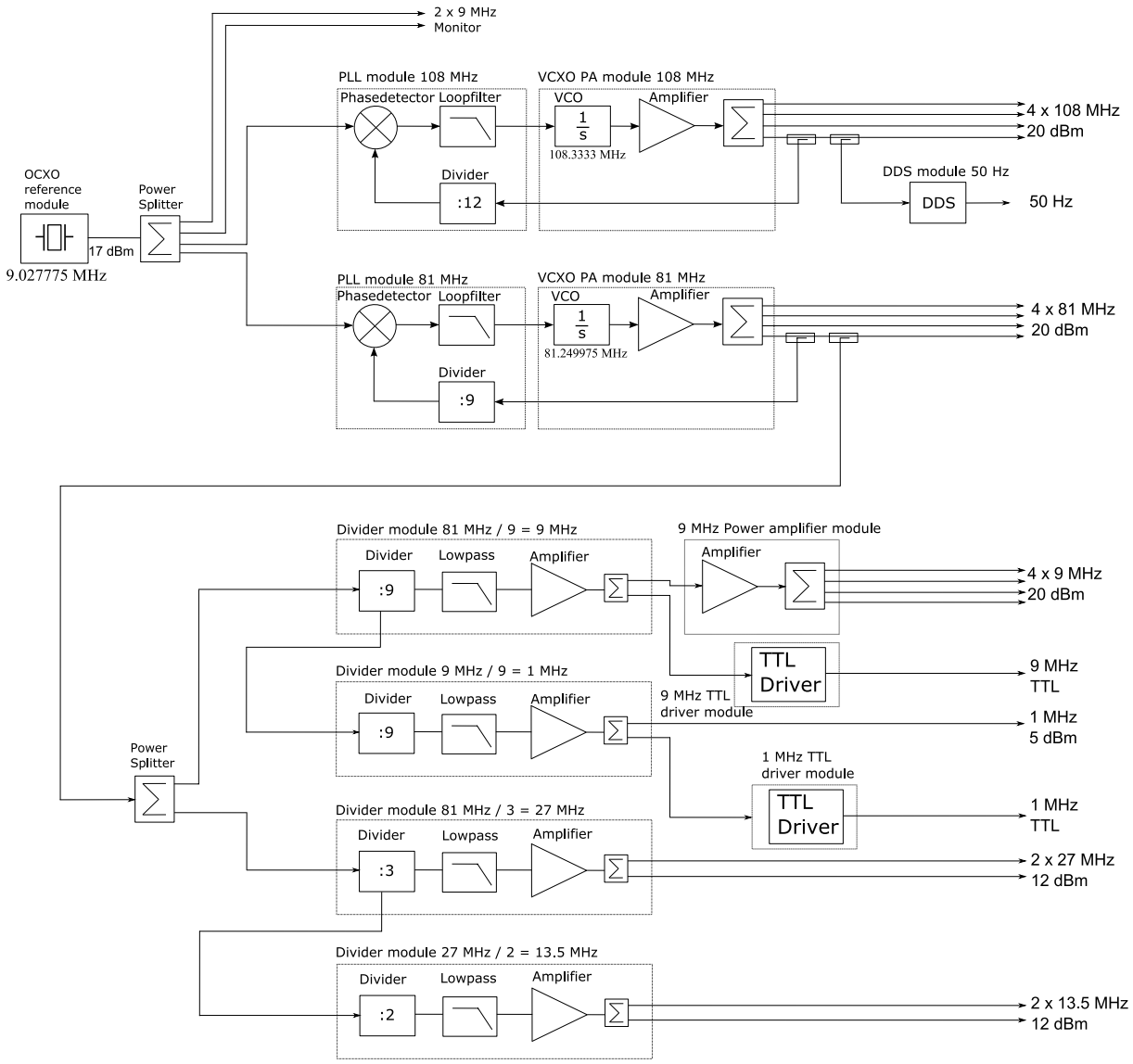

Figure 12: Low Power Part Overview

4.2.1 OCXO reference module

The reference module is an ovenized crystal oscillator stabilized in temperature to minimize the temperature dependent frequency deviations of the output signal. A minimization of this temperature dependence will in return lead to an improved long term stability. Figure 13 shows a thermostat that stabilizes the temperature of the crystal.

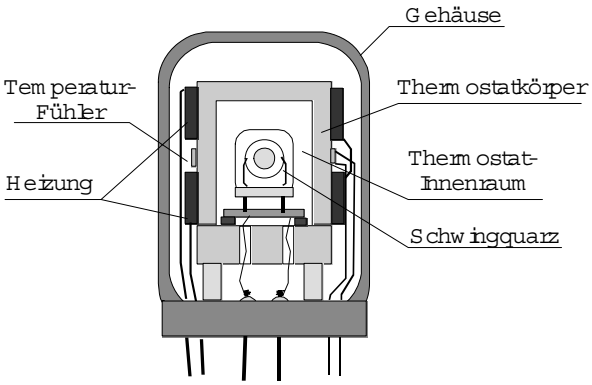

Figure 13: Setup of thermostat [13]

The thermostat is composed of a thermostat chamber (Thermostatkammer) that includes the crystal or even the complete oscillator, the case for the thermostat (Thermostatkörper), the temperature sensor (Temperaturfühler), and the control circuit shown in figure 14.

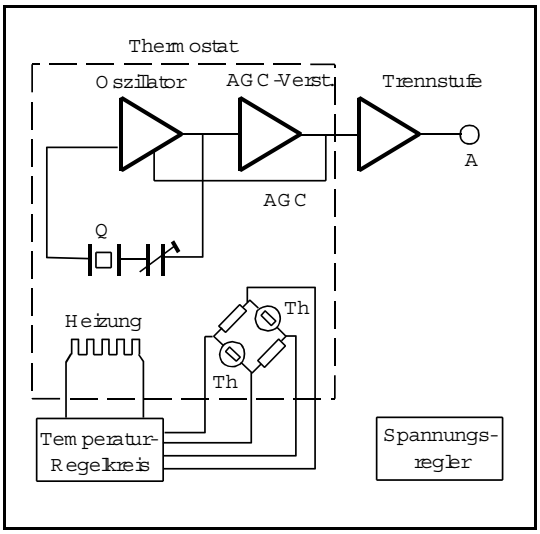

Figure 14: Control circuit to stabilize temperature [13]

For a detailed description refer to [13].
For the Master Oscillator an OCXO from WENZEL ASSOCIATES has been chosen. In order to obtain an operability of the module it needs a certain warm up time (figure 15).

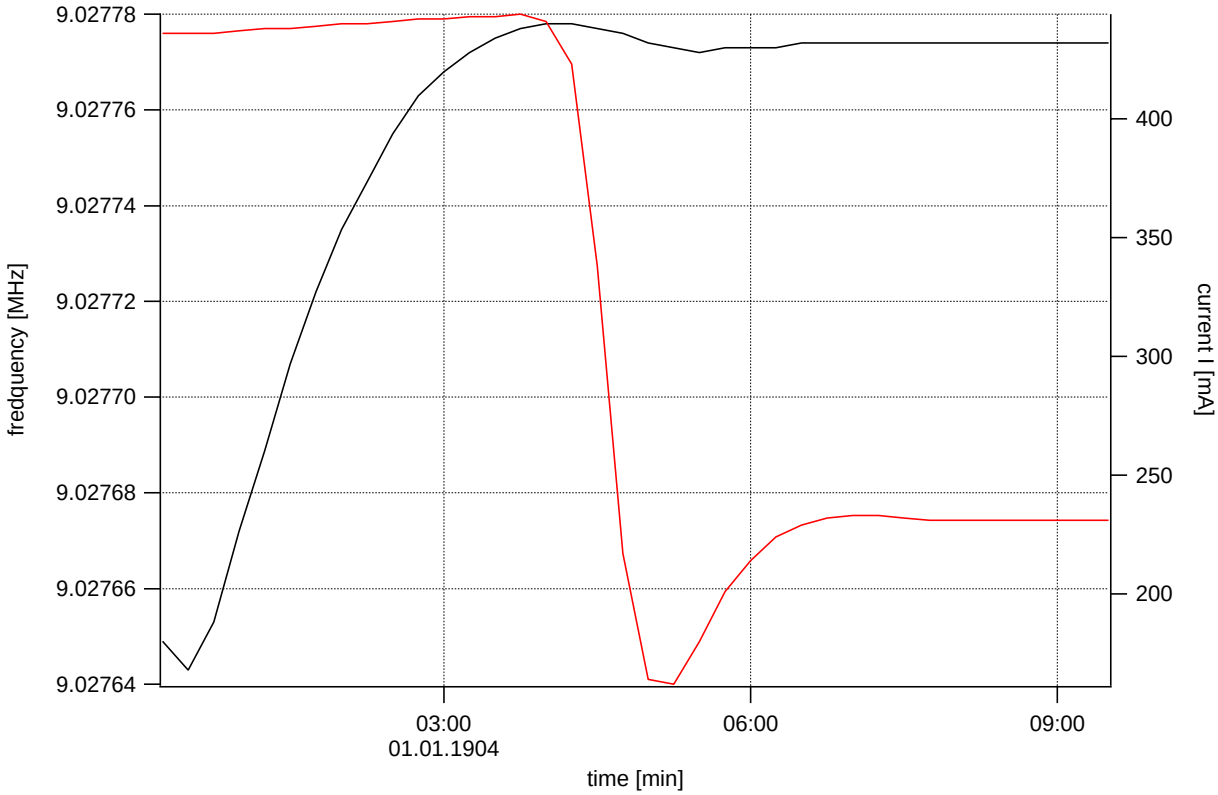

Figure 15: Warm up of OCXO and current consumption, $V_{tune} = 5\ V$

After warm up time the module can operate at its nominal frequency f = 9.027775 MHz with a tuning voltage of $V_{tune} = 5V$. The temperature stability after 10 minutes warmup due to datasheet [3] is $\frac{\Delta f}{f} = 10^{-8}$. The aging after 30 days of operation is 10^{-9}. The module can also be detuned by a tuning voltage $V_{tune} = 5V$ in its frequency to correct for potential deviation of the reference frequency after a long operating time or also in order to synchronize to an external reference source. The tuning voltage ranges from $0\ V < V_{tune} < 10\ V$. The frequency dependence of the tuning voltage is sketched in figure 16. The tuning sensitivity is $K_{VCO} = 5\ \frac{Hz}{V}$.

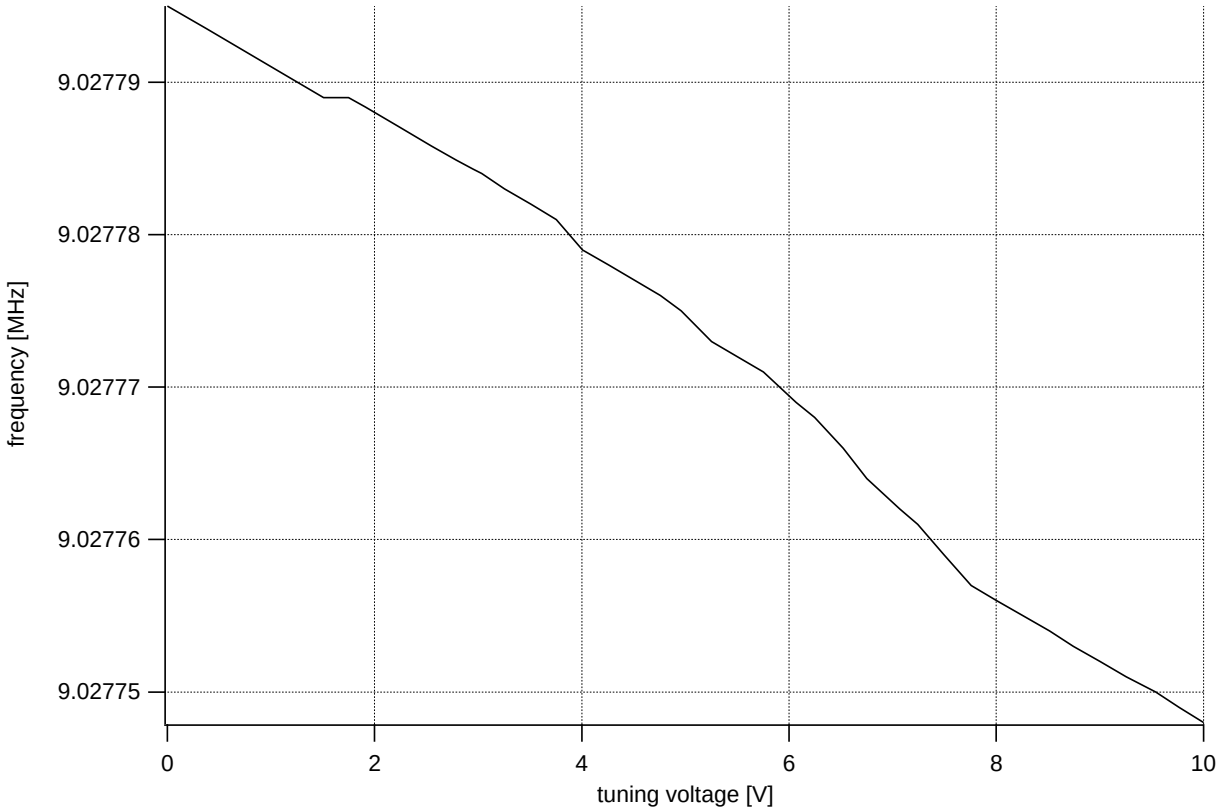

Figure 16: Tuning slope of reference module

The short term stability is specified in terms of phase noise and the datasheet values from the OCXO module are listed in table 2.

offsetfrequency [Hz]	SSB Phasenoise [dBc/Hz]
1	-105
10	-135
100	-150
1000	-155
10000	-162
100000	-164
1000000	-164

Table 2: Phase noise reference module

The phase noise contribution of the reference to the various ouputs will be considered in the following section 4.2.2.

4.2.2 The 81 MHz and 108 MHz phase locked loops

The phase locked loops for 81 MHz and 108 MHz are composed of the reference OCXO at 9.027775 MHz, a phasedetector, a loopfilter and a frequency divider and of the VCXO's at 81 MHz and 108 MHz respectively (figure 17).

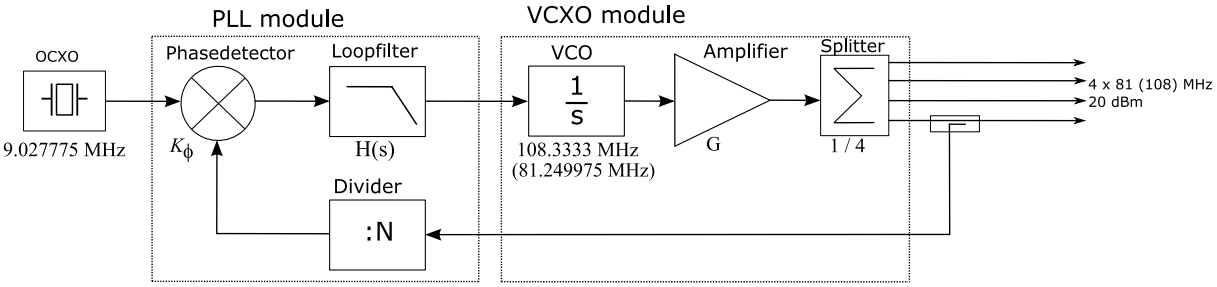

Figure 17: Phase locked loop for 81 MHz and 108 MHz VCXO's

The VCXO modules contain a fifth overtone tunable crystal oscillators with very low phase noise characteristics and an additional amplifier to deliver the required output power. The output amplifier is inside the loop so drifts of the amplifier will be compensated for. The closed loop transfer function reads

$$G_{CL}(s) = \frac{G_{OL}(s)}{\left(1 + \frac{G_{OL}(s)}{n}\right)}, \tag{24}$$

where N is the division ratio in the feedback of the phase locked loop and G_{OL} is the open loop transfer function that reads

$$G_{OL}(s) = \frac{K_\phi \, K_{VCO} \, H_{LF}(s)}{s}, \tag{25}$$

with loop parameters K_ϕ the phasedetector constant, K_{VCO} the voltage controlled oscillator gain and $H_{LF}(s)$ the loopfilter transferfunction that will be discussed later.

The phasedetector and frequency divider:

The phasedetector and frequency divider are combined in one integrated circuit HMC440 from Hittite [10]. The phasedetector has a differential output ND and NU and the frequency divider is programmable with values from 1 to 32. For the 81 MHz PLL a division factor of N = 9 and for the 108 MHz PLL a factor of N = 12 is chosen to obtain in both cases a comparison frequency of 9.027775 MHz.
The phasedetector will add its internal residual phase noise what is not considered in the model introduced in section 2.4. A phasedetector that shows significantly worse phase noise characteristics as compared to the reference OCXO at the 9.027775 MHz input signal would limit the minimum phase noise transport through the PLL. The phasenoise of the phasedetctor is sketched in figure 18.

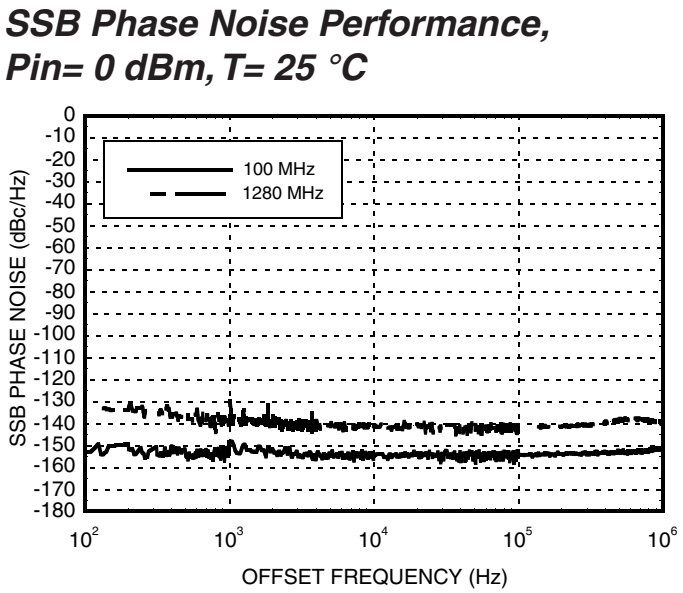

Figure 18: Single sideband phase noise HMC440 [10]

The phasedetector has a noise floor of -150 dBc/Hz at an offsetfrequency of 100 Hz which is smaller than the phase noise of the reference OCXO. In this case the additional noise of the phasedetector is neglectible.

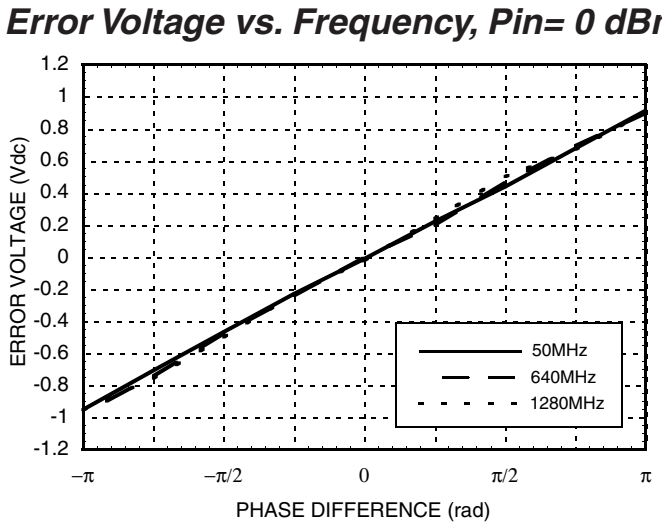

Figure 19: Sensitivity of HMC440[10]

The phasedetector constant K_ϕ is also a parameter that is part of the loop design. The sensitivity K_ϕ can be extracted from figure 19 and has a value of $\frac{1.8\ V}{360°}$.

81 MHz VCXO characteristics tuning slope, tuning sensitivity and phase noise:

These characteristics are essential for designing a stable operating phase locked loop and will enter the phase noise simulation in section 4.2.2 and the stability of the loop in section 4.2.2.

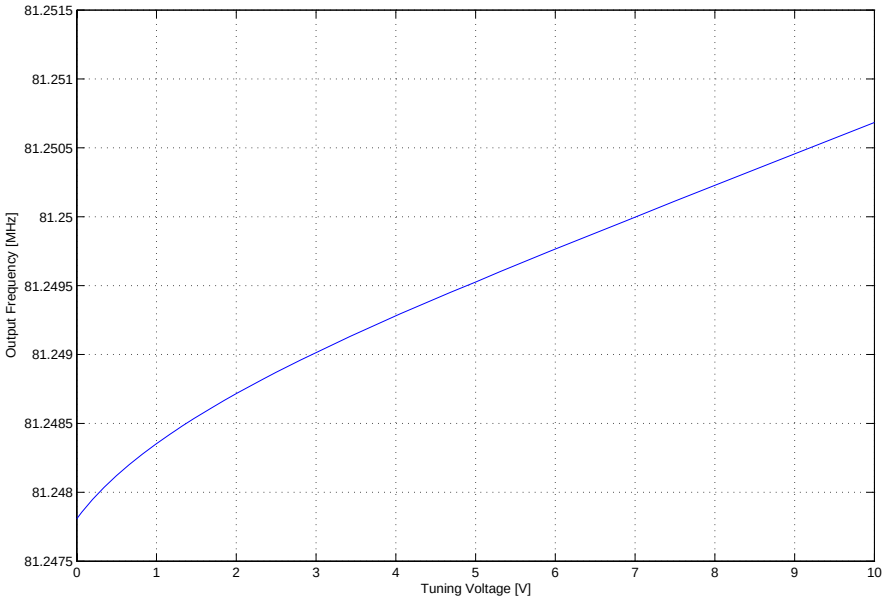

Figure 20: Tuning slope of 81 MHz VCXO

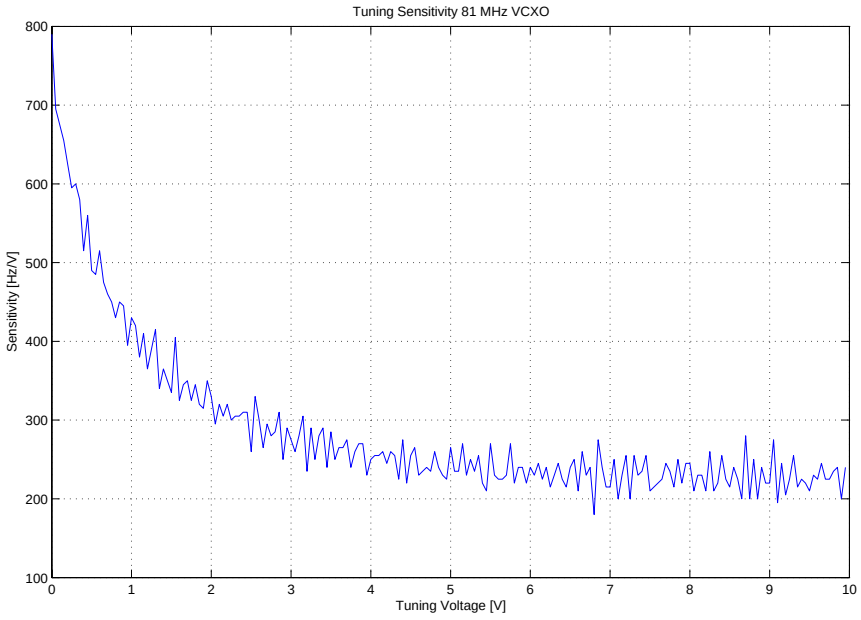

Figure 21: Tuning sensitivity of 81 MHz VCXO

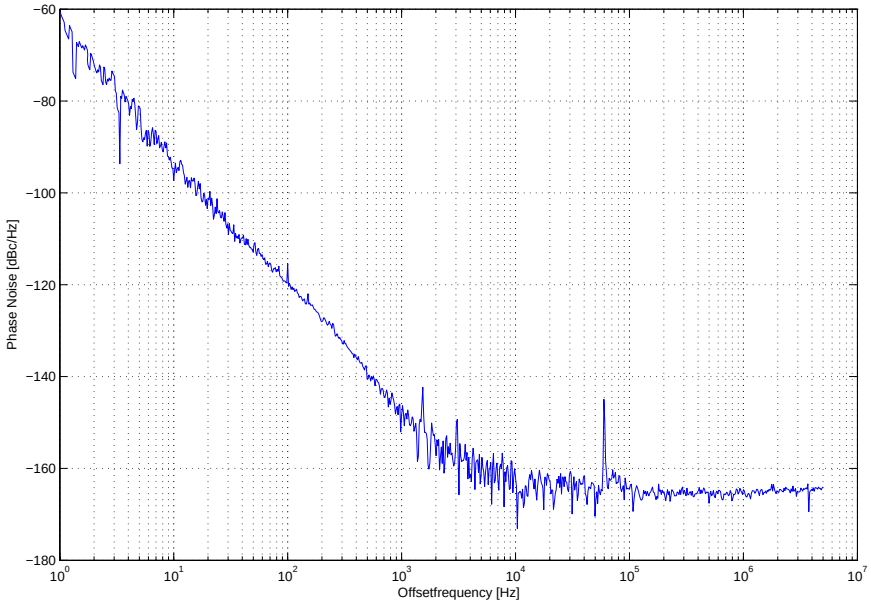

Figure 22: Phase noise of freerunning 81 MHz VCXO

108 MHz VCXO characteristics tuning slope, tuning sensitivity and phase noise:

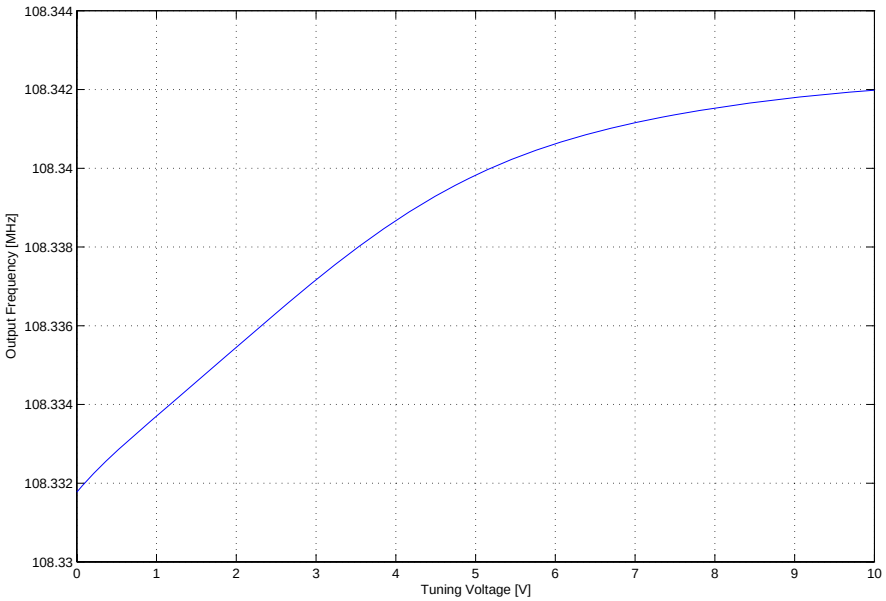

Figure 23: Tuning slope of 108 MHz VCXO

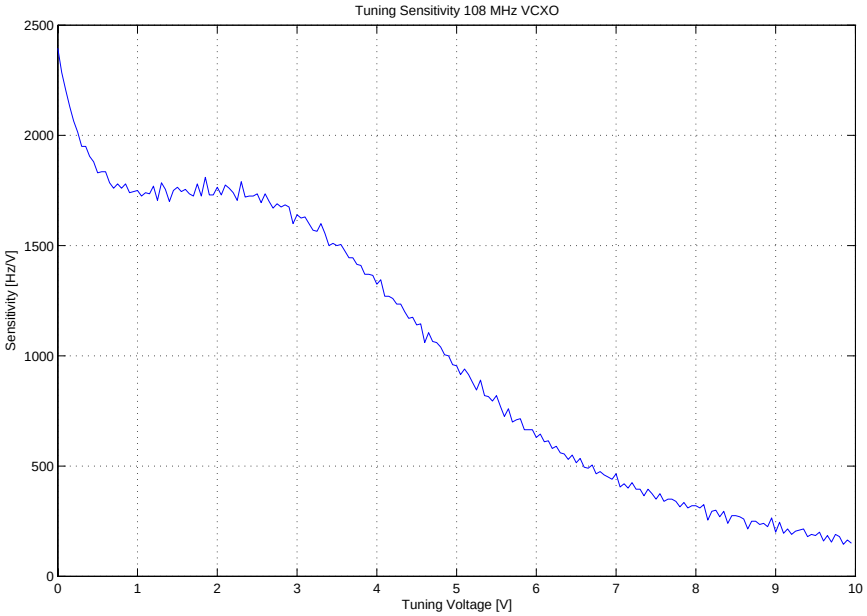

Figure 24: Tuning sensitivity of 108 MHz VCXO

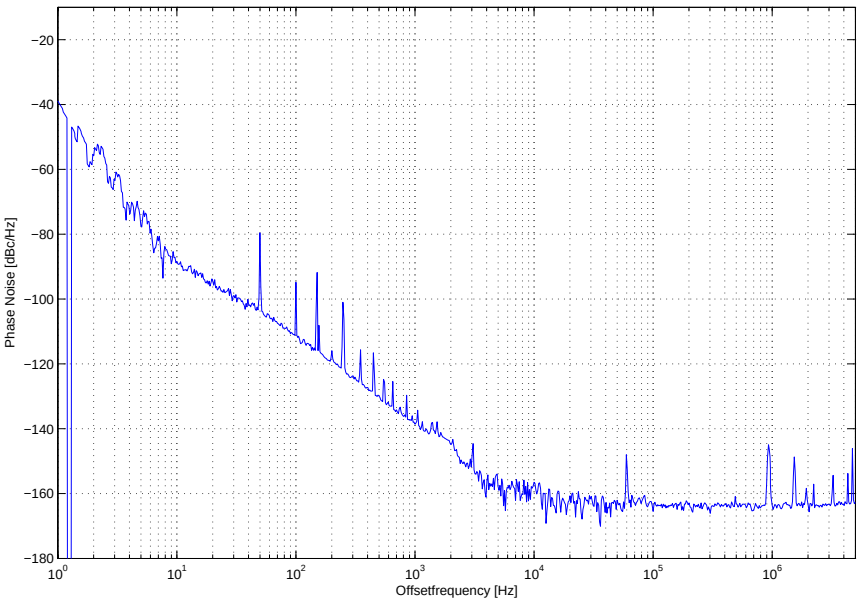

Figure 25: Phase noise of freerunning 108 MHz VCXO

A summary of the tuning sensitivity K_{VCO} and the phase noise of the VCXO's is given in table 3.

	81 MHz VCXO	108 MHz VCXO
K_{VCO}	250 Hz/V [15]	1.75 kHz/V [16]
10	-95	-88
100	-120	-105
1000	-148	-135
10000	-163	-160
100000	-165	-163

Table 3: VCXO parameters

Loopfilter circuit and transfer function $H_{LF}(s)$:

The loop filter $H_{LF}(s)$ is realized as a second order integrator with the transfer function

$$H_{LF}(s) = \frac{1 + sT_2}{sT + s^2TT_3}. \tag{26}$$

The timeconstants T, T_2, T_3 refer to the circuit 26 and read: $T = R_1C_1$, $T_2 = R_3C_1$ and $T_3 = R_5C_3$. The circuit is a differential configuration using an operation amplifier LT1028 [17] to integrate the phase errors of the differential output of the phasedetector HMC440 [10]. The circuit for the loop filter in the 81 MHz PLL is sketched in figure 26.

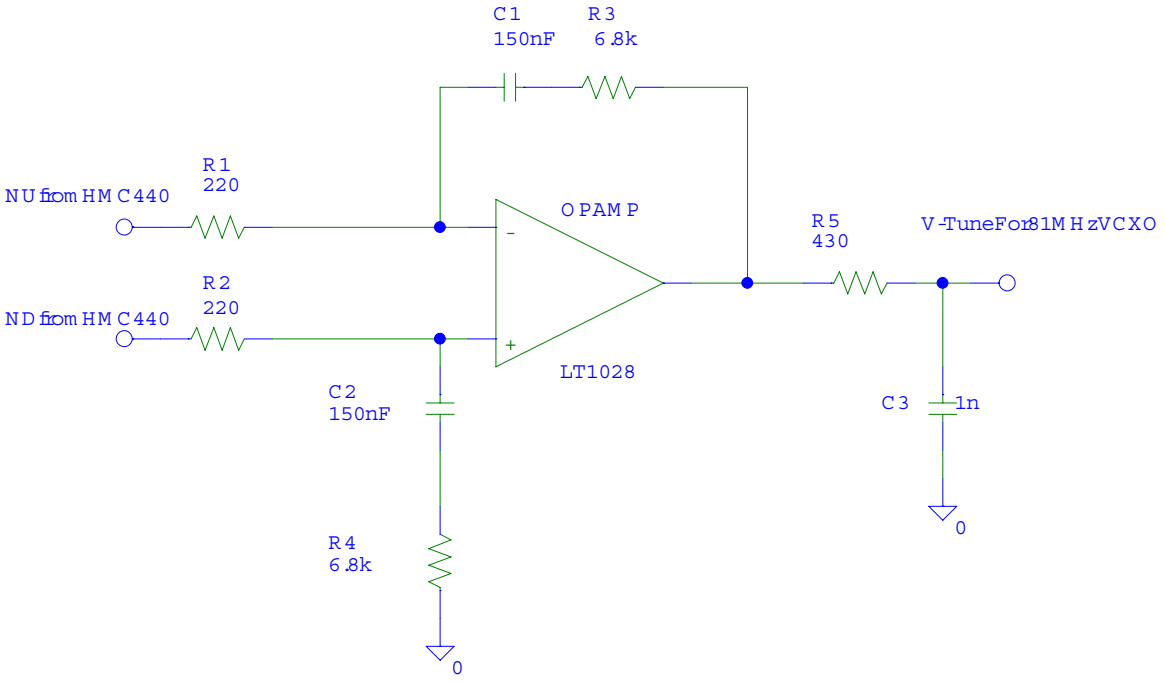

Figure 26: Loopfilter of 81 MHz PLL

[15] for a tuning voltage of $V_{tune} = 1V$ to obtain an outputfrequency of 108.3333 MHz
[16] for a tuning voltage of $V_{tune} = 5.5V$ to obtain an outputfrequency of 81.249975 MHz

The circuit for the loop filter in the 108 MHz PLL is sketched in figure 27.

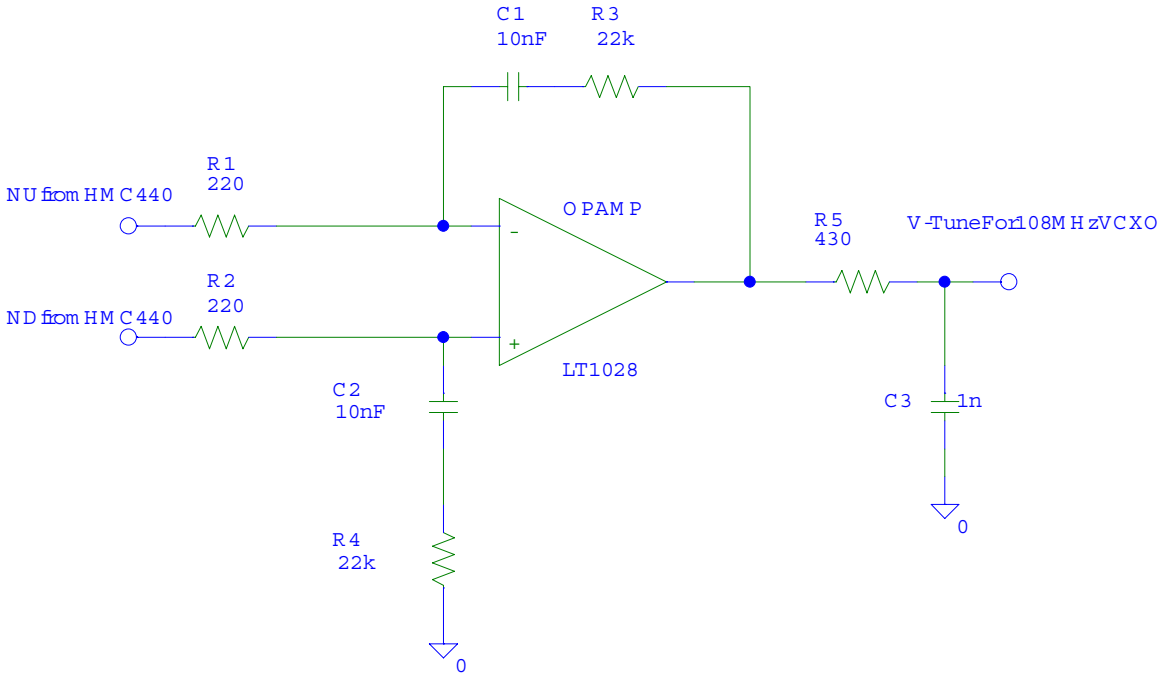

Figure 27: Loopfilter of 108 MHz PLL

The transfer function with the corresponding parameters of the operation amplifier circuit are used for the simulation of transport of phase noise through the PLL in the next subsection and the stability consideration in the after next section of the PLL.

Phase noise transported through the 81 MHz PLL:

Due to the phase noise model in section 2.4 the reference and VCO phase noise contribute to the overall phase noise. The reference phase noise is lowpass filtered and the VCO phase noise is highpass filtered.
The reference phase noise of the OCXO from table 2 has been taken for simulating the phase locked loop output phase noise[17] and therefore is scaled by a factor of N = 9 [18] due to equation 2.3.
The loop filter transfer function as seen by the reference OCXO and the VCXO are sketched in figures 28 and 29.

[17] minimum input frequency for measurement instrument is 10 MHz so phase noise data for reference from datasheet had to be taken

[18] in a logarithmic scale 20 dB

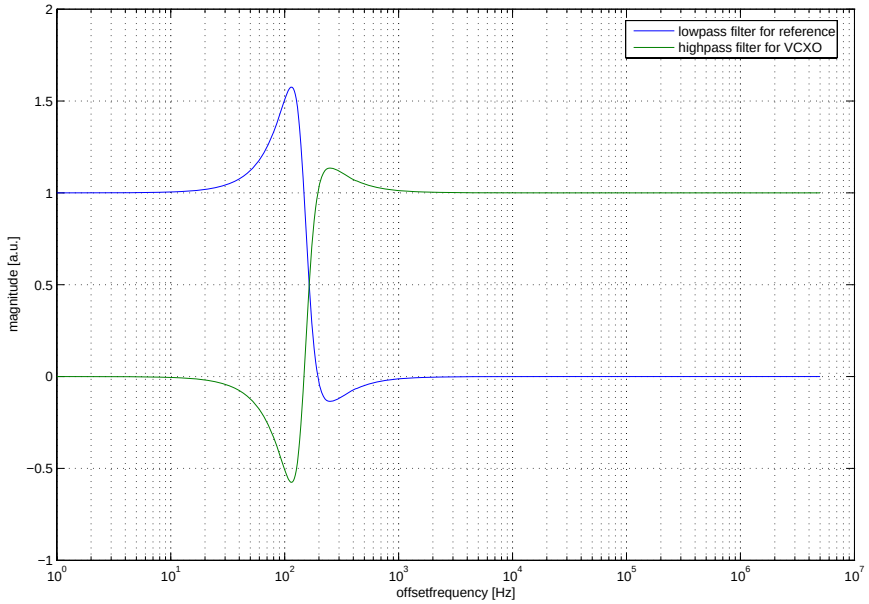

Figure 28: Lowpass as "seen" by the 9.027775 MHz OCXO reference and highpass filtered as seen by the 81 MHz VCXO

The loop filter as simulated shows a cutoff at around 100 Hz what could be verified by the measurement of phase noise of the closed loop 81 MHz VCXO as depicted in figure 29.

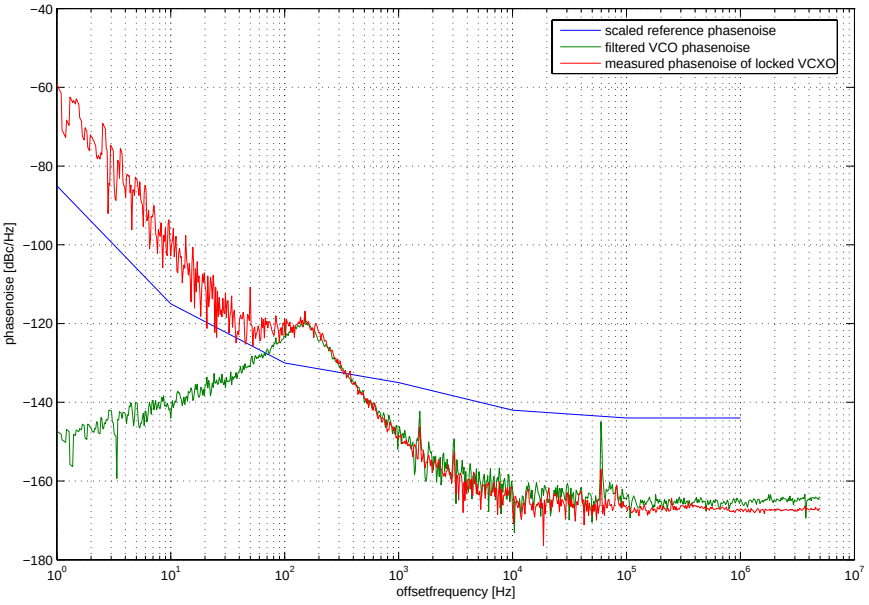

Figure 29: 81 MHz phase locked loop with highpass filtered 81 MHz VCXO phase noise

The scaled reference phase noise deviates by roughly 10 dB up to 15 dB from measurements of closed loop phase noise. A discussion of deviations will be given in the summary. The integrated timing jitter[19] for measured phase noise at 81 MHz is around 70 fs[20].

[19] 10 Hz. . . 1 MHz

[20] measured without correlation

The same has been done for the 108 MHz VCXO with a factor N = 12 and is sketched in figures 30 and 31.

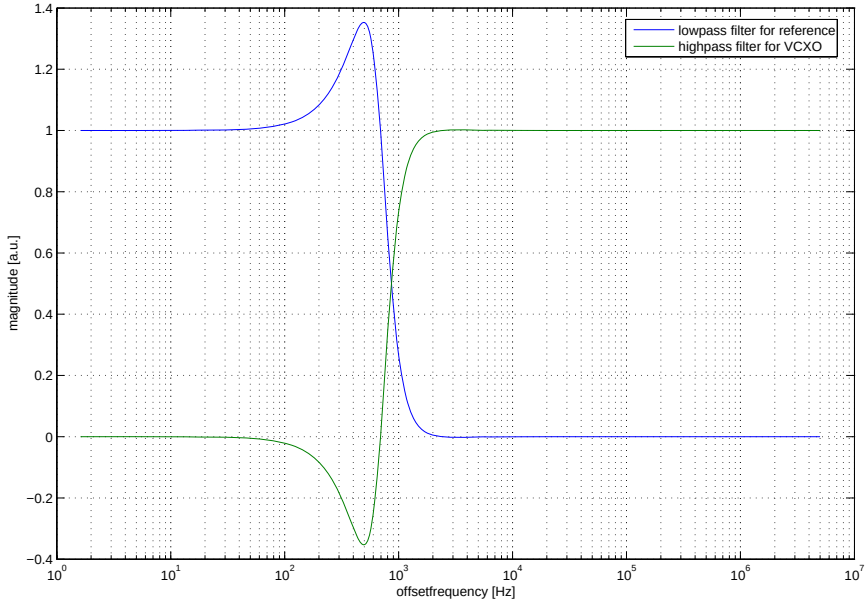

Figure 30: Lowpass as "seen" by the 9.027775 MHz OCXO reference and highpass filtered as seen by the 108 MHz VCXO

The loop filter as simulated shows a cutoff at around 1 kHz what could be verified by the measurement of phase noise of the closed loop 108 MHz VCXO as depicted in figure 31.

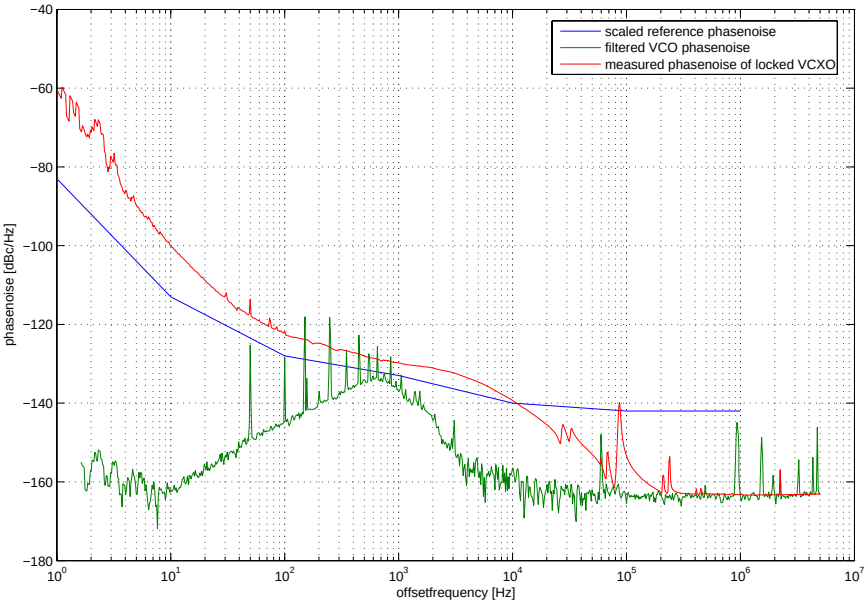

Figure 31: 108 MHz phase locked loop with highpass filtered 108 MHz VCXO phase noise

The scaled reference phase noise again deviates by roughly 10 dB up to 15 dB from mea-

surements of closed loop phase noise. The integrated timing jitter[21] for measured phase noise at 81 MHz is around 75 fs[22].

Stability of loops:

The stability limit for control loops such as phase locked loops is when the open loop gain $G_{OL} > 1$ when the phase shift of the open loop reaches $\phi = -180°$.

This means that phase errors will no longer be subtracted but added in the feedback of a control loop due to the change of sign introduced by the phaseshift bigger than $\phi = -180°$. Amplitude and phase of open loop transfer functions of the phase locked loops for 81 MHz and 108 MHz have been simulated. The results are shown in figure 32 for the 81 MHz loop and in figure 33 for the 108 MHz loop respectively.

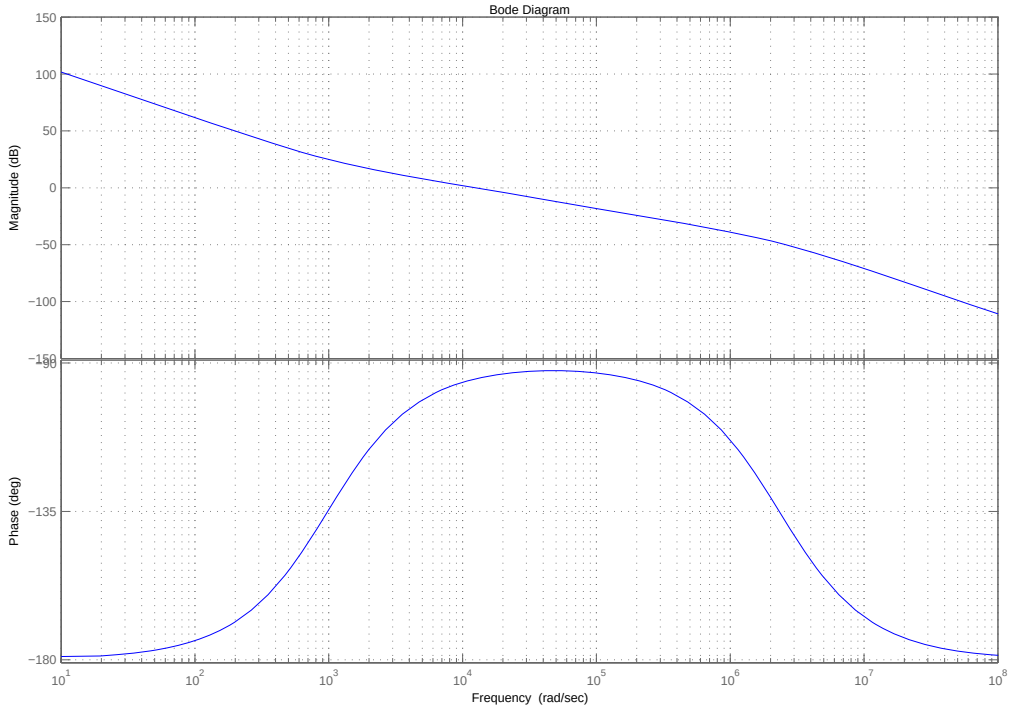

Figure 32: Magnitude and phase of closed loop transfer function of 81 MHz PLL

[21] 10 Hz. . . 1 MHz

[22] measured without correlation

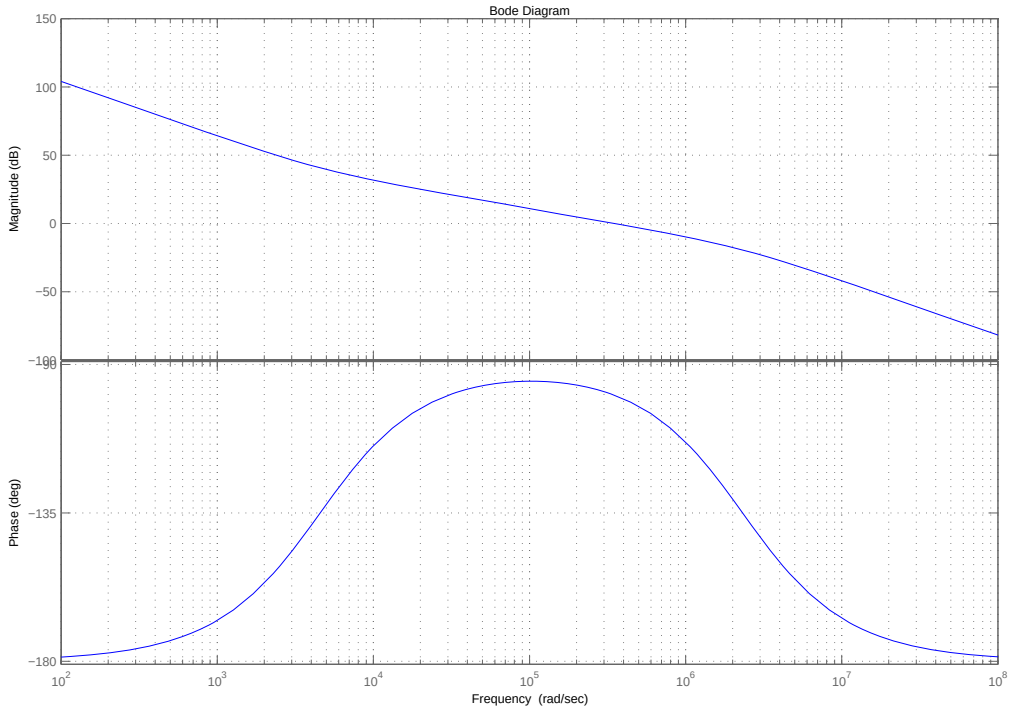

Figure 33: Magnitude and phase of closed loop transfer function of 108 MHz PLL

Both loops are stable and have a phasemargin $\phi_{margin} > 60°$ [23].

Harmonics at the output of 81 MHz and 108 MHz loop:

The harmonics of the outputs at 81 MHz and 108 MHz are measured with a spectrum analyzer. The requirement document [21] requires a distance of harmonics $< 25\ dB$ below the carrier. A summary of harmonic distance in the outputs is given in table 63.

fundamental	1st harmonic [dBc]	2nd harmonic [dBc]	3rd harmonic [dBc]
81MHz	<35	<40	<40
108MHz	<35	<35	n.m.[24]

Table 4: Table of harmonics in outputs from locked 81 MHz and 108 MHz VCXO

[23] point at which the gain decreased to $|G| = |1|$
[24] n.m.= not measured

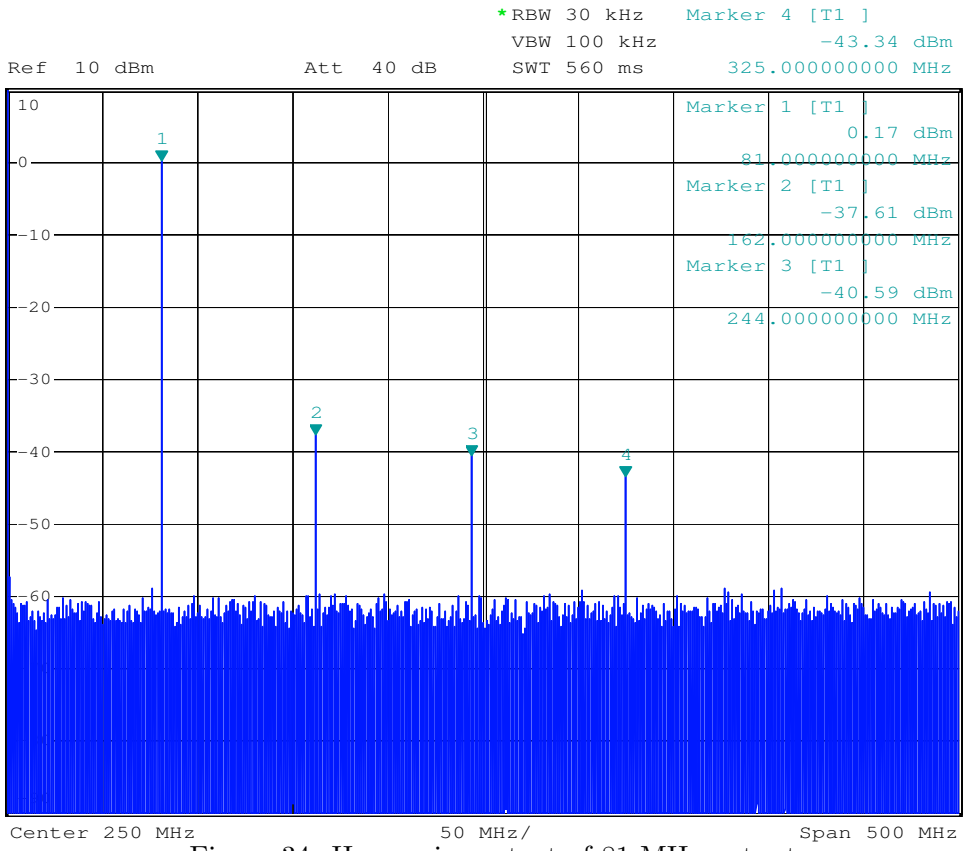

Figure 34: Harmonic content of 81 MHz output

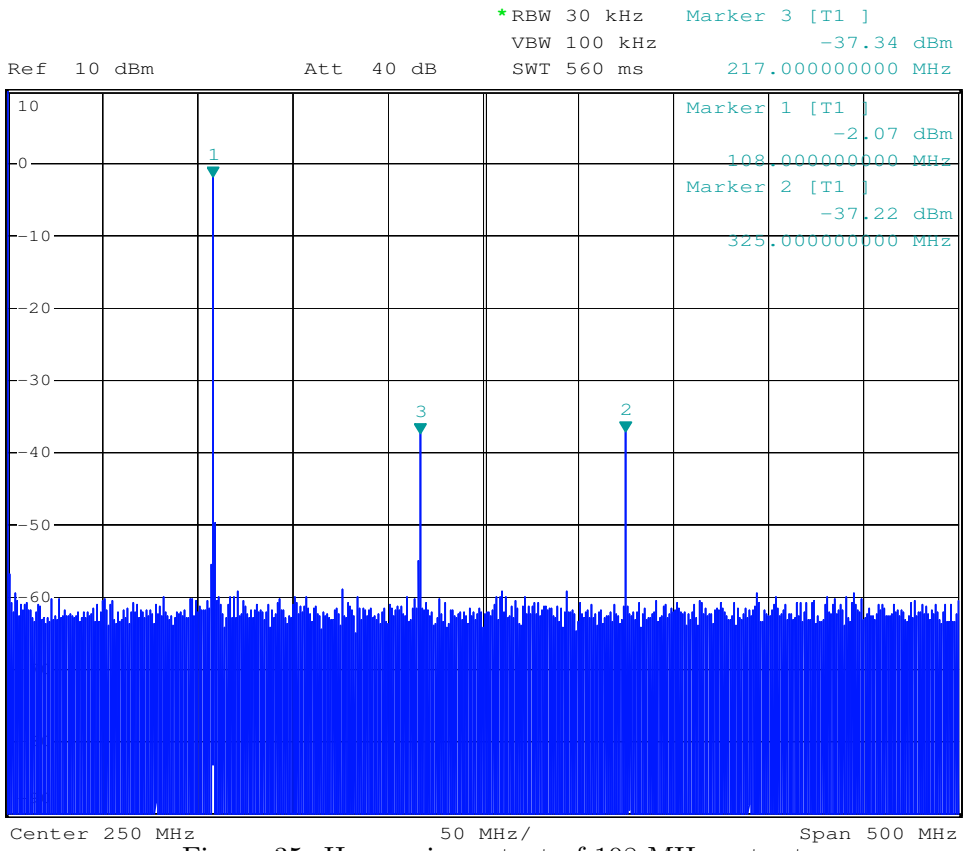

Figure 35: Harmonic content of 108 MHz output

4.2.3 Divider modules for 27 MHz, 13.5 MHz, 9 MHz, 1 MHz

The divider modules that generate the frequencies 27 MHz, 13.5 MHz, 9 MHz and 1 MHz are programmable with division factors from 0 to 32. The chip used here is the HMC394 [9]. The divider is a device based on ECL technology that features two independent outputs of the divided signal. One signal is low pass filtered and amplified to deliver the powers listed in table 1. The other output is inverted and serves as a reference signal for the other module as sketched in figure 12. The phase noise limits of the chip are sketched in figure 36.

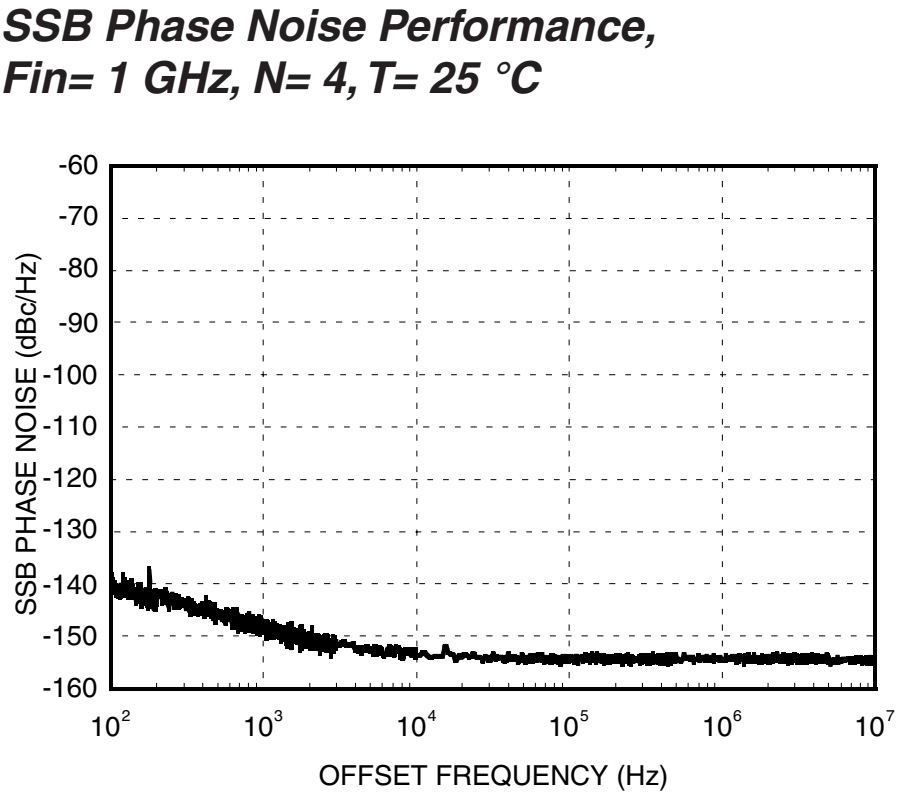

Figure 36: Phase noise floor of divider module [9]

The phase noise at offsetfrequency 100 Hz is -140 dBc/Hz, at 1 kHz -150 dBc/Hz and a phase noise floor of -155 dBc/Hz is reached at 10 kHz offset frequency. The phase noise of the outputs 27 MHz and 13.5 MHz is sketched in figure 37 and 38.

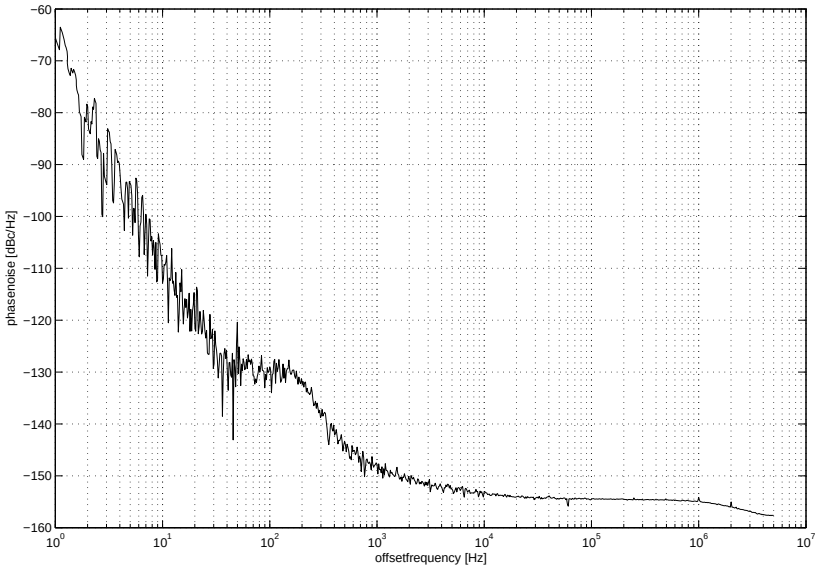

Figure 37: Phase noise at 27 MHz divider output

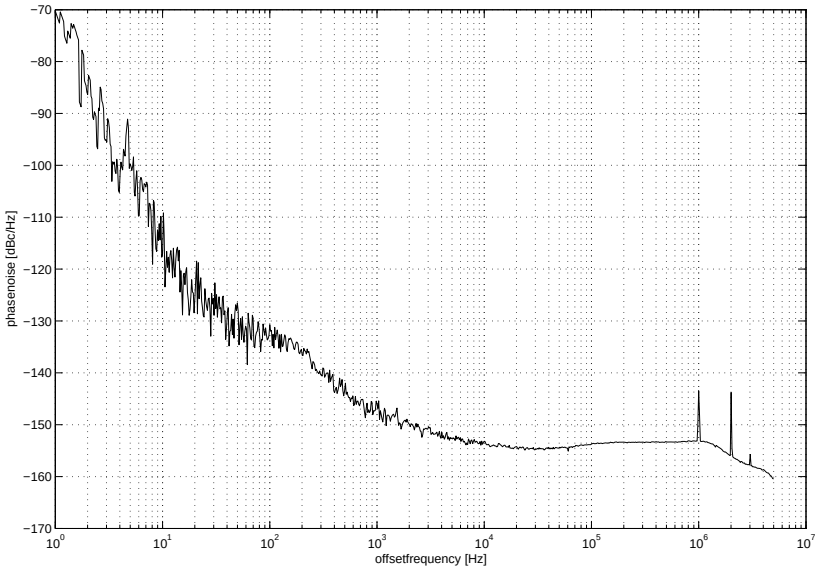

Figure 38: Phase noise at 13.5 MHz divider output

The integrated timing jitter ΔT_{rms}[25] for the outputs of the divider modules are 170 fs and 385 fs for the 27 MHz and for 13.5 MHz respectively [26].

Harmonics at the output of 27 MHz, 13.5 MHz and 9 MHz:

The harmonics of the divider outputs at 9 MHz, 13.5 MHz and 27 MHz are measured with a spectrum analyzer. The requirement document [21] requires a distance of harmonics $< 25\ dB$ below the carrier. A summaray of harmonics is given in table 5.

[25] from 10 Hz ... 1 MHz

[26] phase noise of 9 MHz and 1 MHz outputs could not be measured with E5052

fundamental	1st harmonic [dBc]	2nd harmonic [dBc]	3rd harmonic [dBc]
9MHz	<40	<60	<70
13.5MHz	<45	n.m.[27]	n.m.
27MHz	<50	n.m.	n.m.

Table 5: Table of harmonics in 9 MHz, 13.5 MHz and 27 MHz divider module

4.2.4 9 MHz Power amplifier

The output of the 81 MHz / 9 divider module is amplified again to obtain four outputs with approximately 20 dBm for each output. The output versus input power characteristic of one of the four outputs is sketched in figure 39.

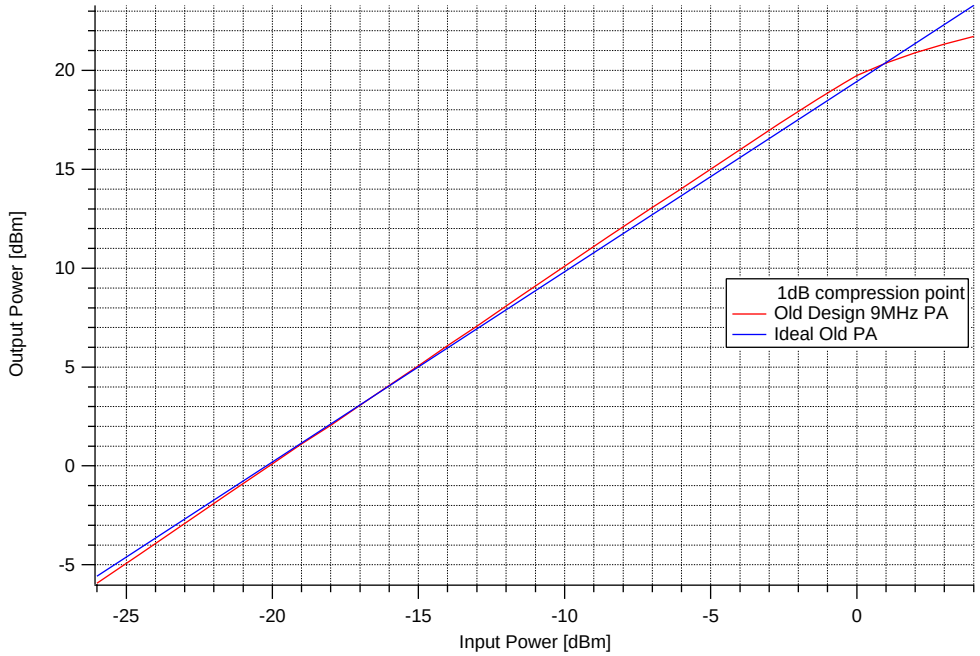

Figure 39: 1 dB compression point of 9 MHz module

An operation in the linear regime of the amplifier is recommended and minimizes the phase deviation from the input to the output. An input power of 0 dBm is sufficient to deliver an output power of approximately 20 dBm for each output.

4.2.5 TTL drivers for 9 MHz and 1 MHz TTL signal

For timing purposes in the facility two outputs with TTL signal levels at 9 MHz and 1 MHz are required [21]. The TTL driver input and output signals are sketched in figures 40 and 41. The input signals are delivered from the divider modules.

[27] n.m. = not measured

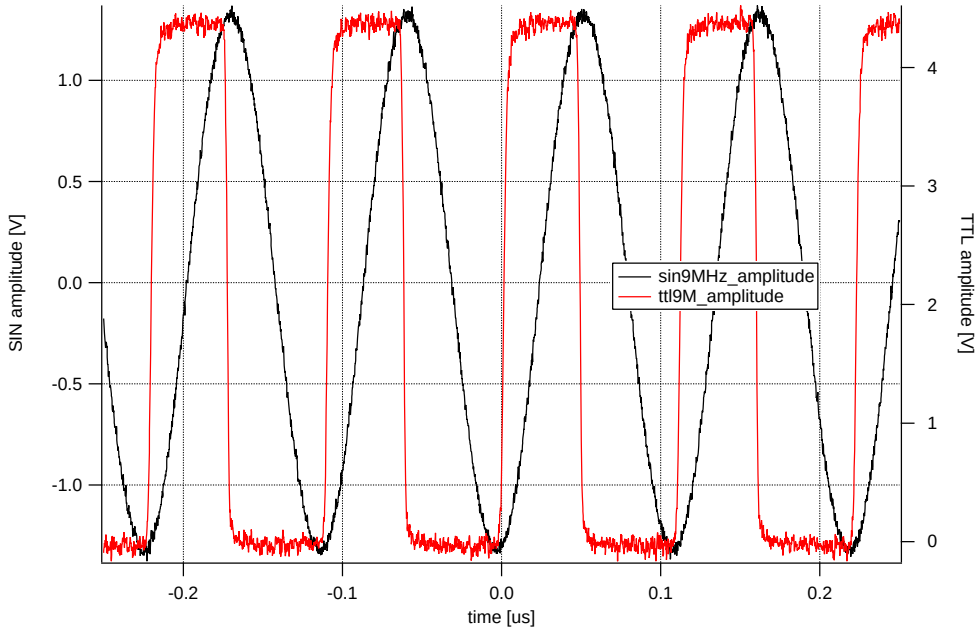

Figure 40: 9 MHz sinusoidal input - and TTL output signal

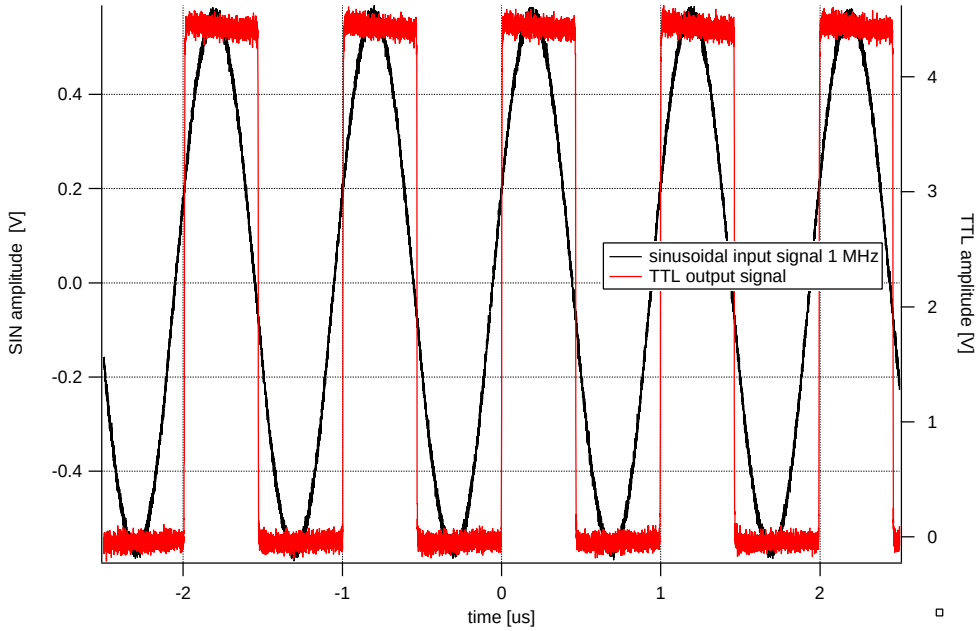

Figure 41: 1 MHz sinusoidal input - and TTL output signal

The additional jitter of these drivers have not been investigated up to this point.

4.2.6 Direct digital synthesis of 50 Hz

The input signal for the DDS module is coupled out from the 108 MHz VCXO module and generates the signal sketched in figure 42.

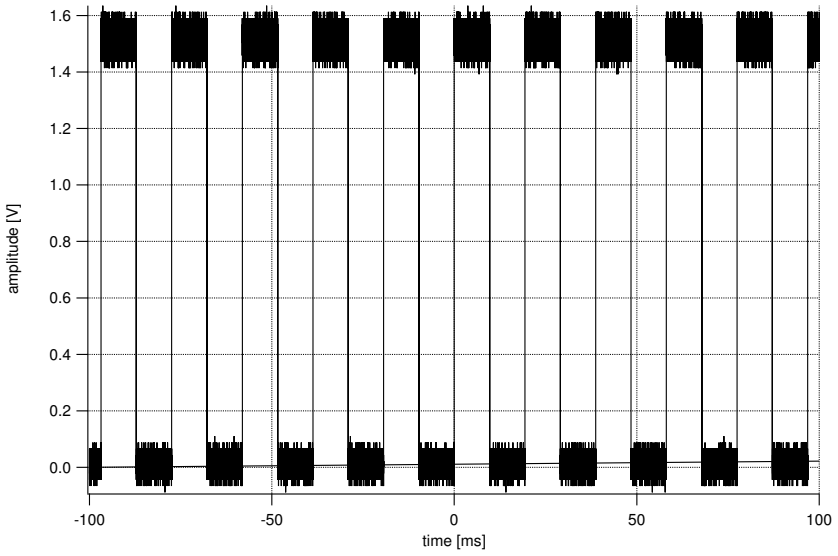

Figure 42: Output signal 50 Hz DDS

The additional jitter of the DDS has also not been investigated up to this point.

4.3 1.3 GHz and 2.856 GHz phase locked loops

This section introduces the 1.3 GHz and the 2.856 GHz phase locked loops. The 1.3 GHz uses an N = 16 integer division of the output frequency while the 2.856 GHz uses a fractional N division of the output frequency. Both phase locked loops have a reference frequency of 81 MHz that is taken from the locked VCXO from the low power part (see figure 4.1).

4.3.1 1.3 GHz PLL

The 1.3 GHz phase locked loop is realized in two alternative setups that are discussed in the following. The first setup (sketched in figure 43) makes use of a mixing scheme to generate the 1.3 GHz output frequency [28].

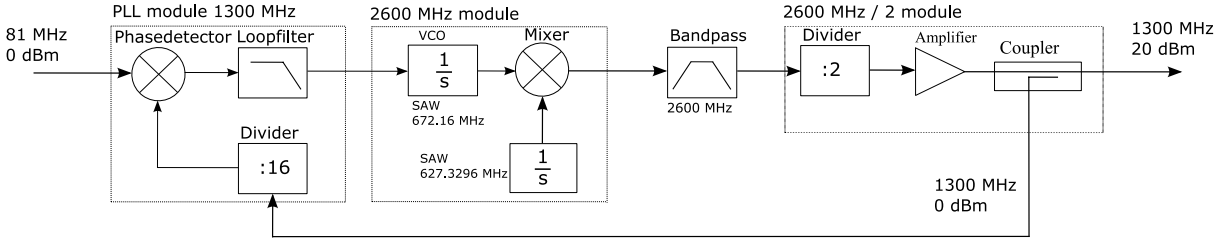

Figure 43: 1.3 GHz PLL with SAW at 627.3296 MHz mixing with SAW at 672.16 MHz

The tuning slope and tuning sensitivity of the freerunning 2600 MHz module are sketched in figure 44 and 45.

[28] the sum frequency of the second harmonics of two SAW (Surface Acoustic Wave) oscillators at 672.16 MHz and 627.3296 MHz generate a frequency at 2.598979 GHz that is divided by a factor of 2 and finally is amplified again

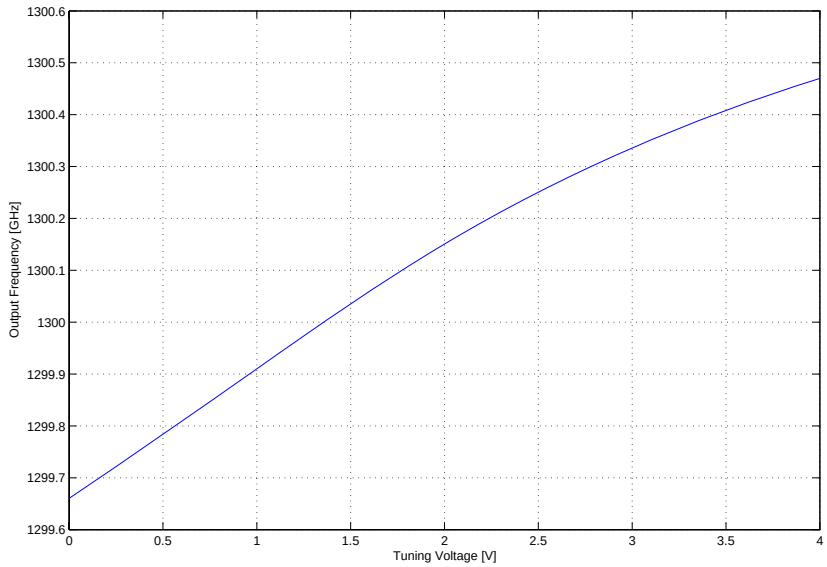

Figure 44: Tuning slope of SAW oscillator

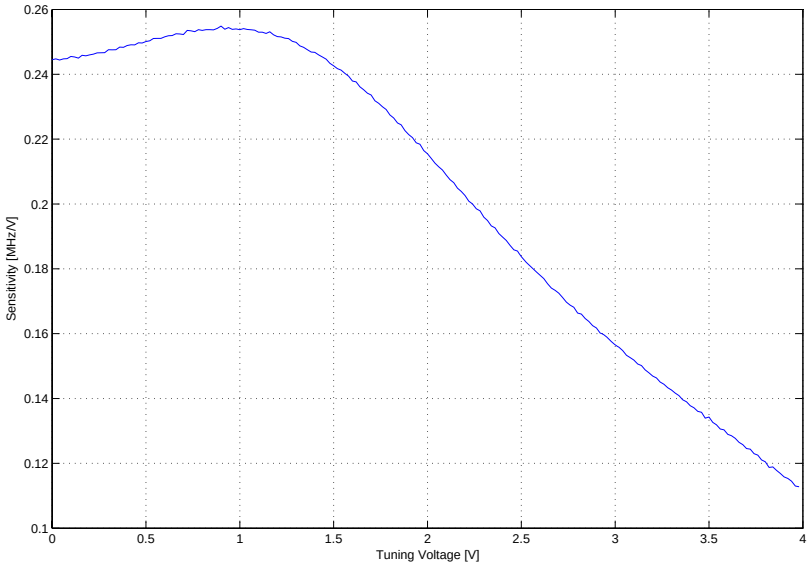

Figure 45: Sensitivity of SAW oscillator

The components used in the phase locked loop module are the same as the ones used in the VCXO PLL modules in section 4.2.2.

Loop transfer functions and measured phase noise:

The loop transfer functions for lowpass filtered reference phase noise and highpass filtered SAW phase noise has been simulated and is sketched in figure 46.

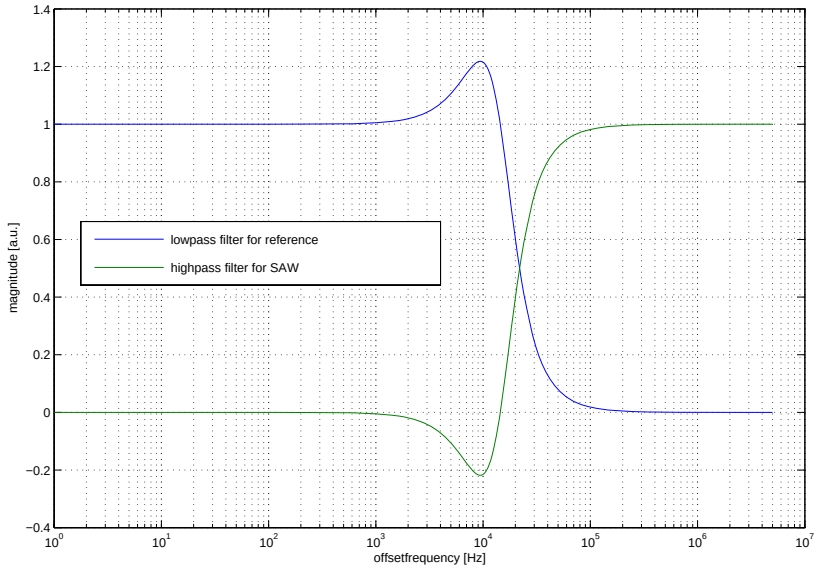

Figure 46: Transfer functions as "seen" by the reference and the SAW

The filter shows a cut off at around 11 kHz what could be verified by measurements of the closed loop phase noise what is sketched in figure 47. For the loop filter parameter estimation the reference phase noise of the locked 81 MHz VCXO has been scaled by a factor of N = 16 [29], the phase noise of the freerunning SAW oscillator, the simulated locked loop phase noise and the measured locked loop phase noise are sketched in figure 47.

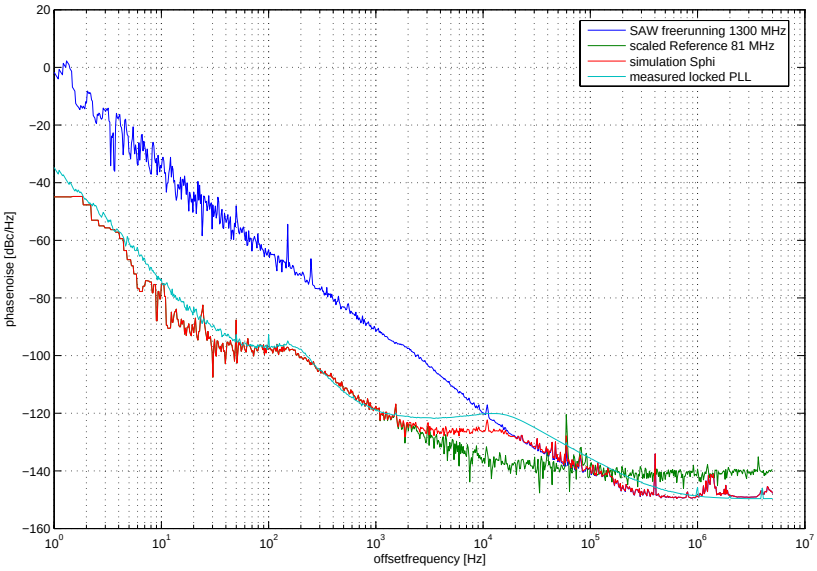

Figure 47: Measured and simulated phase noise in locked SAW phase locked loop

The integrated timing jitter[30] is 70 fs.

[29] roughly 24 dB
[30] integration bandwidth from 10 Hz...1MHz

Stability of SAW loop:

The stability has been investigated and the magnitude and phase of the closed loop transfer function are sketched in figure 48.

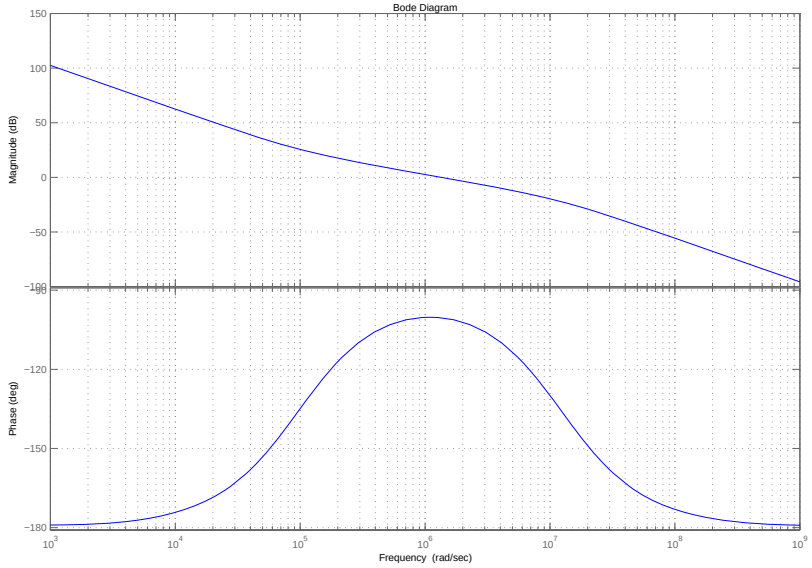

Figure 48: Simulation of stability of closed loop with SAW

The loop has a phase margin of $> 60°$ and therefore is stable.
An alternative design is given with a single module oscillator a socalled DCSO[31]. The setup is sketched in figure 49.

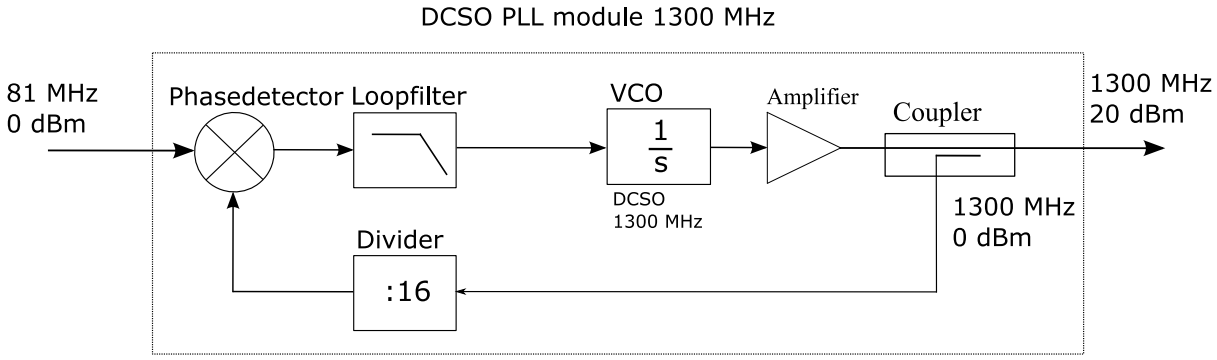

Figure 49: DCSO module phase locked loop

The resonator oscillates at 1.3 GHz and is tunable as depicted in figure 50 and has a sensitivity as depicted in figure 51.

[31] a ceramic SAW replacement resonator from SYNERGY MICROWAVE

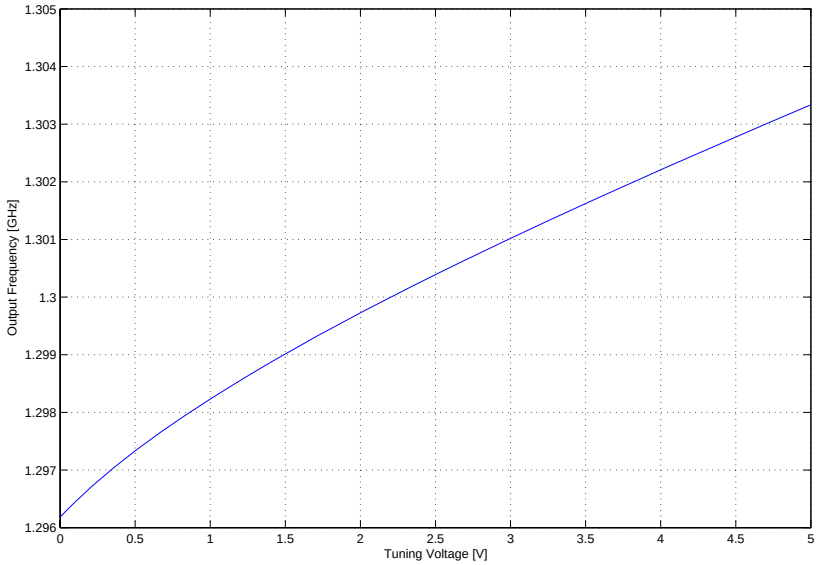

Figure 50: DCSO slope

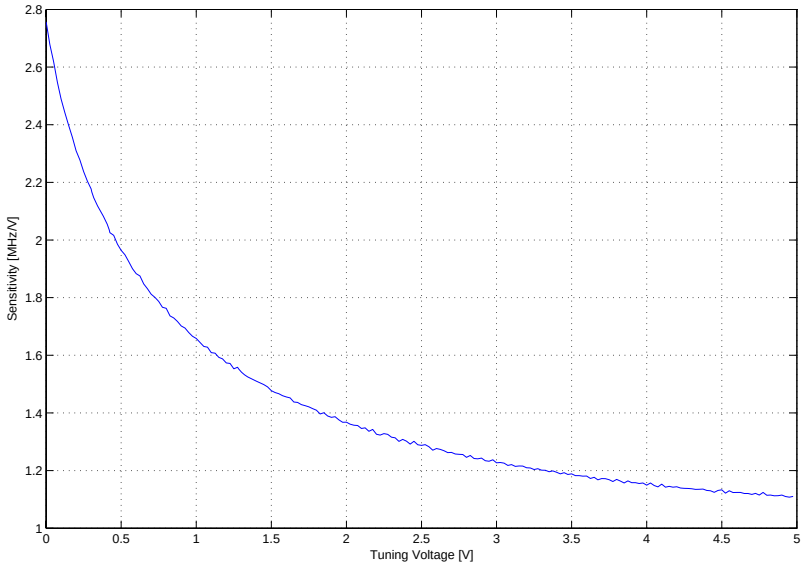

Figure 51: Sensitivity of DCSO

Loop transfer functions and measured phase noise:

The loop transfer functions for lowpass filtered reference phase noise and highpass filtered DCSO phase noise has been simulated and is sketched in figure 52.

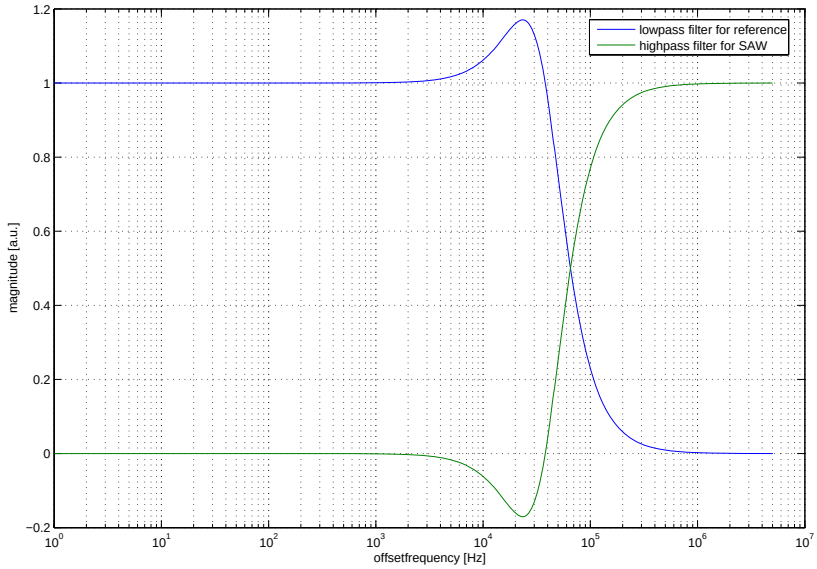

Figure 52: Transfer functions as "seen" by the reference and the DCSO

The filter shows a cut off at around 50 kHz what could not be verified by measurements of the closed loop phase noise sketched in figure 53. For the loop filter parameter estimation the reference phase noise of the locked 81 MHz VCXO has been scaled by a factor of N = 16 [32], the phase noise of the freerunning DCSO oscillator, the simulated locked loop phase noise and the measured locked loop phase noise are sketched in figure 53.

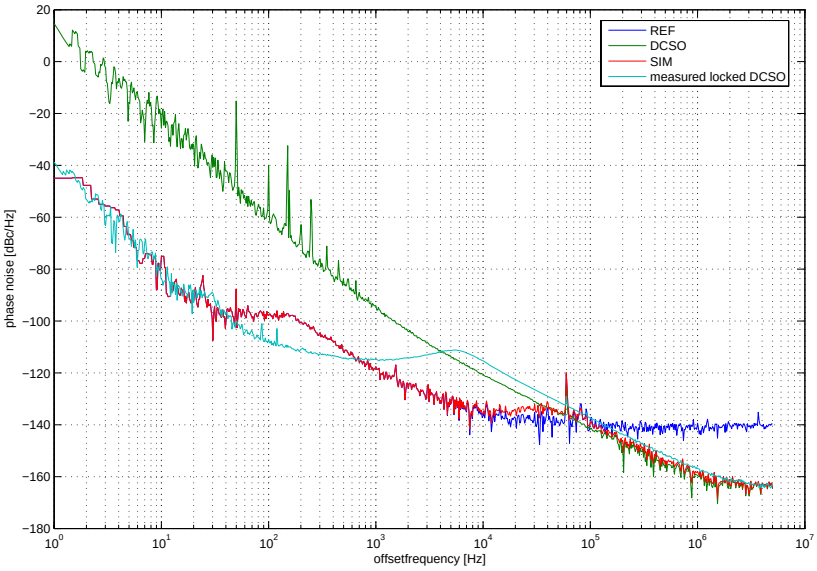

Figure 53: Measured and simulated phase noise in locked DCSO phase locked loop

The integrated timing jitter[33] is 58 fs.

[32] roughly 24 dB
[33] integration bandwidth from 10 Hz...1MHz

Stability of DCSO closed loop:

The stability has been investigated and the magnitude and phase of the closed loop transfer function are sketched in figure 54.The loop has a phase margin of 50° and therefore is stable.

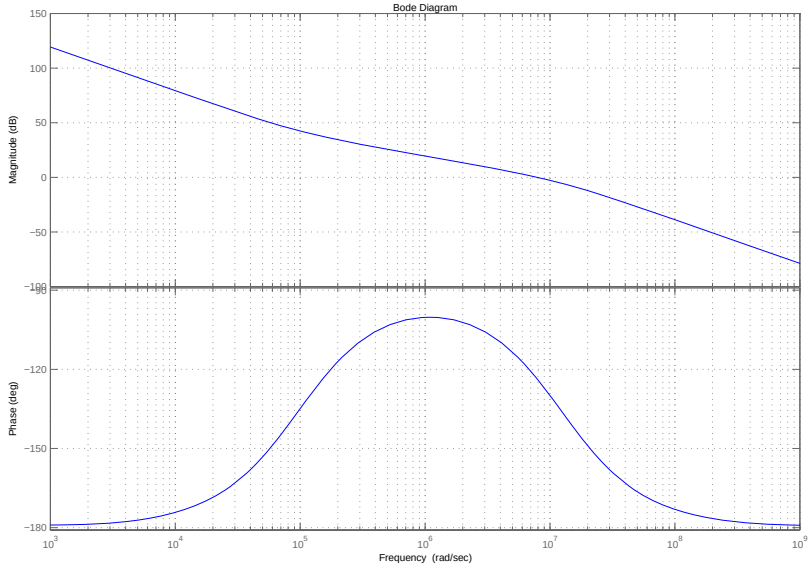

Figure 54: Simulation of stability of closed loop with DCSO

Comparison of locked SAW resonators and DCSO oscillator:

Both setups have integrated timing jitters smaller than 100 fs, while the locked DCSO shows a value that is 12 fs smaller than for the locked SAW oscillator. The reason for this is that an improved phase noise performance of the 81 MHz VCXO reference ha been taken for the measurement. The SAW module has a less tuning sensitivity in the range of 400 kHz / Hz than the DCSO module with 1.4 MHz / V. This might be disadvantageous for the closed loop gain in the case of the DCSO module because the gain of the loop filter than has to be chosen smaller to guarantee a stable operation of the phase locked loop. The higher sensitivity of the DCSO module will as well react more sensitive to voltage fluctuations at the input that finally will modulate the oscillator in a crucial way.

4.3.2 2.856 GHz Fractional N PLL

The deflection cavity LOLA to investigate the bunch lengths of FLASH at DESY operates at 2.856 GHz (2.856001105 GHz) and must be synchronized to the distribution frequency 81.25 MHz. A common PLL using a division ratio of N will lead to unsatisfactorily synchronization errors in frequency and phase. Therefore a fractional N PLL using a the chip ADF4153 from Analog Devices is used with an active loop filter. The parameters of the chip can be programmed via a serial interface from the RS232 port. The PLL characteristics are studied with the goal to minimize the frequency error of the synchronized frequencies and the resulting timing jitter.

The blockdiagram in figure 55 illustrates the entire PLL to synchronize the reference frequency 81.2499997 MHz and the 2.856001105 GHz oscillator.

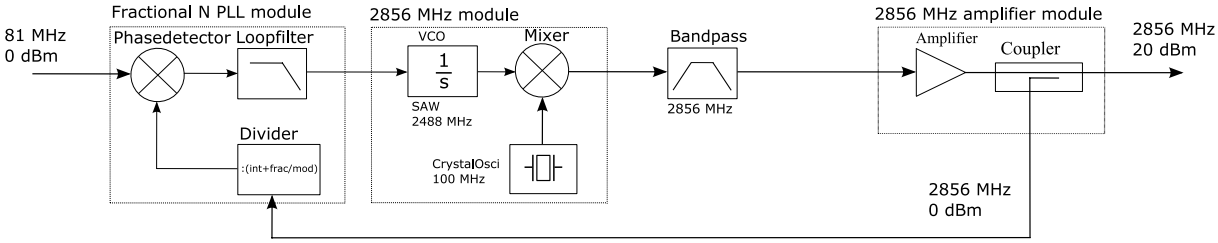

Figure 55: LOLA PLL

The oscillator is generated by mixing the second harmonic at 200 MHz of a high stable crystal oscillator with a SAW (Surface Acoustic Wave) oscillator at 2488 MHz. The mixing product is filtered out with a bandpass filter and amplified in the end. The VCOs characteristics are sketched in figures 56, 57 and 58.

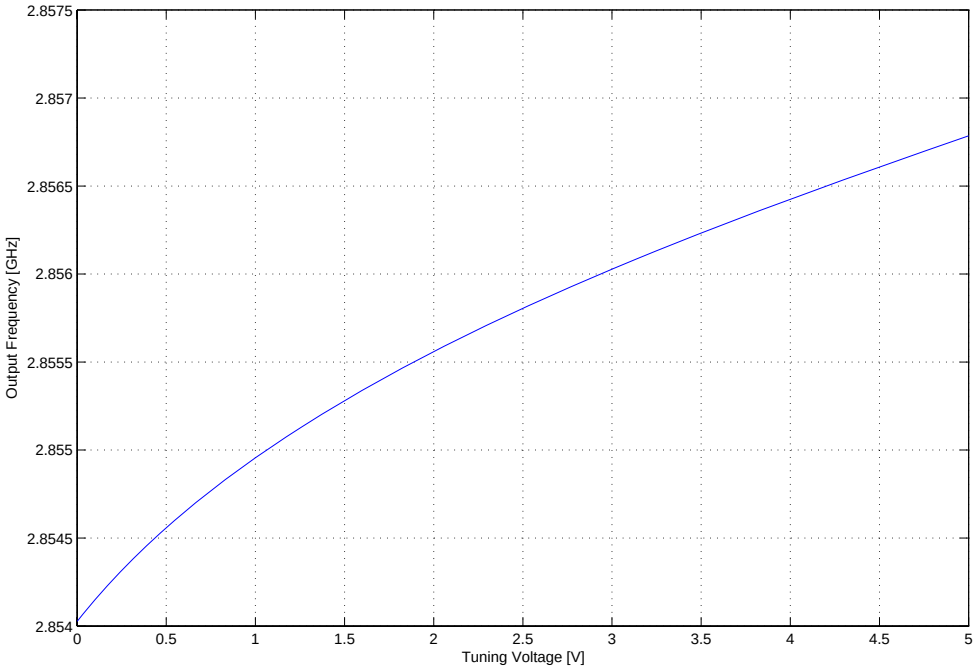

Figure 56: Tuning slope of 2.856 GHz VCO

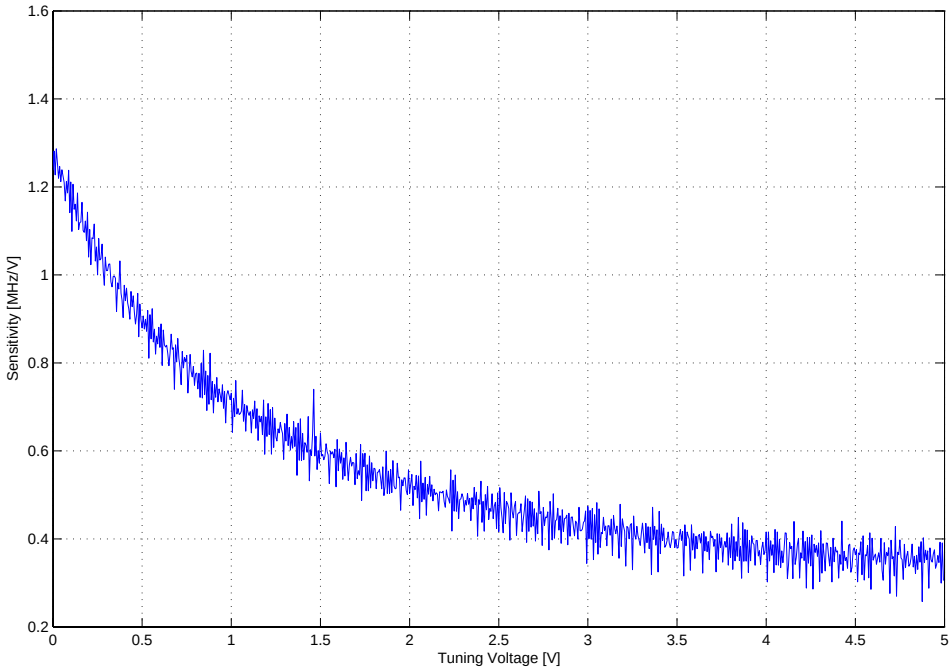

Figure 57: Tuning sensitivity

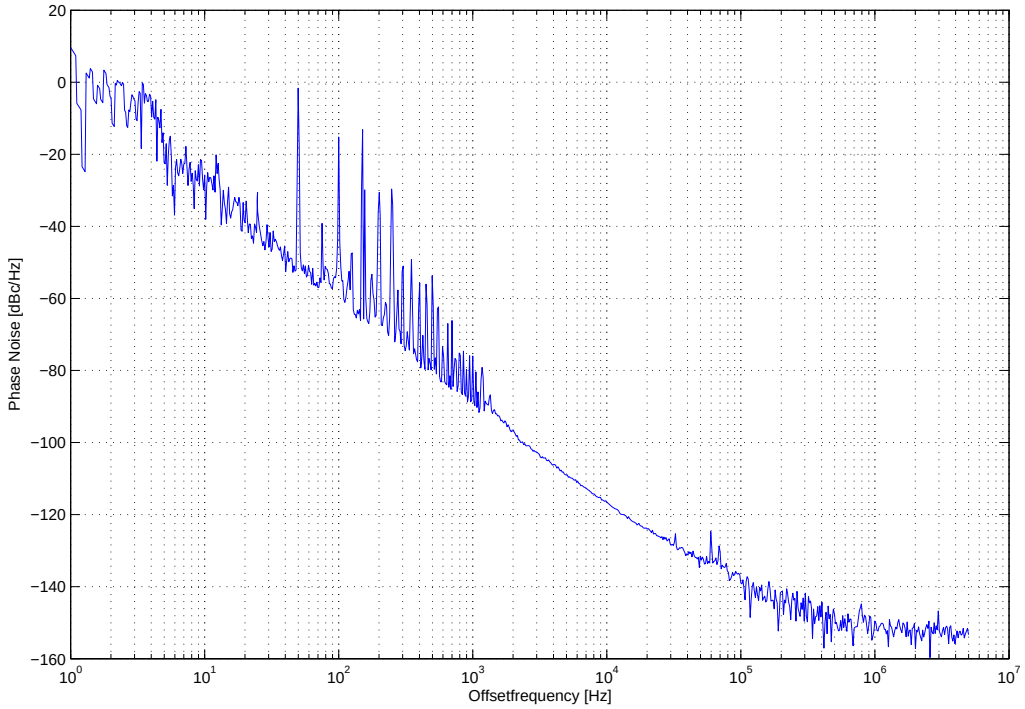

Figure 58: Free running phase noise at 2.856 GHz

Determination of output frequency: The outputput frequency of the entire PLL can be calculated like

$$f_{RF} = PFD\ (\ INT\ +\ FRAC/MOD) \tag{27}$$

where PFD is the phasedetector frequency that reads:

$$PFD = f_{REF}((1 + D) / R) \tag{28}$$

where f_{REF} is the reference frequency and D is a input frequency doubler Bit. The output frequency is adjustable due to equation 27 by the variables

1. R = 0...15
2. INT = 0...511
3. FRAC = 0...4095
4. MOD = 0...4095

and a doubler Bit D to double the input frequency[34]. Doubler Bit D is set off and R divider is set to 4. An example for programming the registers is put in the appendix.
Loop Filter: The Loopfilter used in the PLL is an active Filter using an operation amplifier as sketched in figure 59.

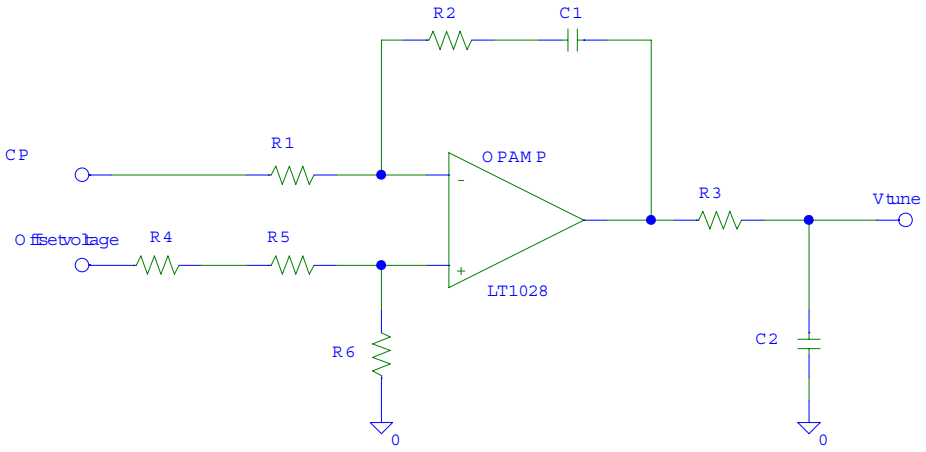

Figure 59: Loopfilter LOLA PLL

The parameters chosen for the Filter here are listed in table 6.

R1	0Ω
R2	5$k\Omega$
C1	10nF
R3	1$k\Omega$
C2	6.8nF
R4[35]	1$k\Omega$
R5	220Ω
R6	1$k\Omega$

Table 6: Loop filter parameters

[34]disabled here
[34]R4, R5 and R6 for putting an offsetvoltage of 1.8 V at positve pin of operation amplifier

Performance of PLL:

For the loop filter parameter estimation the reference phase noise of the locked 81 MHz VCXO has been scaled to 2.856 GHz, the phase noise of the freerunning SAW oscillator at 2.856 GHz, the simulated locked loop phase noise and the measured locked loop phase noise are sketched in figure 60. The integrated timing jitter including the spurs in the spectrum is smaller than 450 fs.

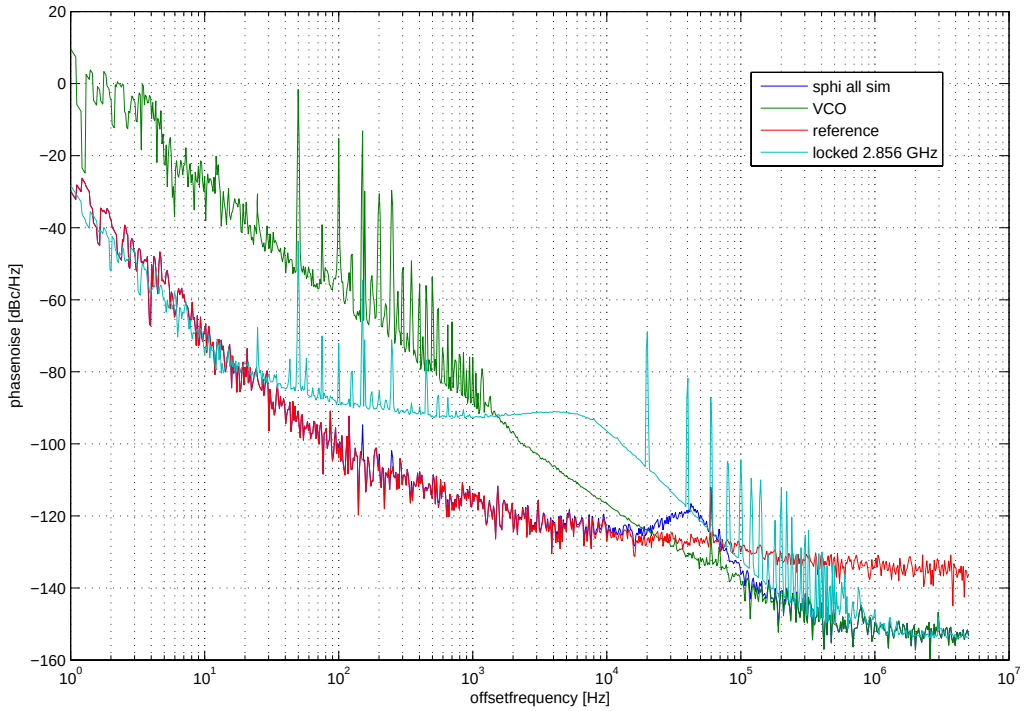

Figure 60: Loop filter estimation and measured phase noise of synchronized 2.856 GHz

4.4 High Power Part for amplification of 81 MHz and 1.3 GHz signals

For the distribution of the signals over distances up to 300 m in the facility the output power of 20 dBm of the main distribution frequencies 81 MHz and 1.3 GHz delivered by the Low Power Part and the 1.3 GHz PLL as shown in figure 4.1 will not be sufficient for long distant tap points due to the attenuation in cables. Therefor additional amplification of these signals is necessary. The signals at 81 MHz and 1.3 GHz will be amplified up to 43 dBm.
The amplifiers should not add drifts exceeding 1 ps at a constant temperature over an operating time of several hours. Up to this point investigations concerning the drifts of amplifier have been made [16] for a 1.3 GHz amplifier using the measurement principle introduced in section 3.2.3. For an ambient temperature change of $3°C$ the drifts at 1.3 GHz are within +/- 1 ps what seems do be promising to meet the design goal of drifts smaller than 1 ps. The drifts shows high correlation with ambient temperature changes. As a consequence a stabilization of ambient temperature in the accelerator environment is unavoidable.

5 Summary and Conclusion

The requirements of generating integrated timing jitters smaller than 100 fs could be met with the 81 MHz and 108 MHz and with the 1.3 GHz phase locked loops using the mixing process and the single DCSO module. The limitations for the integrated timing jitters are highly dominated by the phase noise characeristics of the OCXO 9.027775 MHz reference module but there are deviations from the datasheet phase noise levels and the measured ones[36]. In order to determine the real phase noise at offset frequencies up to 100 Hz of the locked VCXO's at 81 MHz, 108 MHz, 1.3 GHz and the 2.856 GHz PLL the correlation factor of the measurement instrument has to be set to 10000 which is the maximum number N of measurement entering the formula 19. The deviations of measured and simulated loop filters to minimize the integrated timing jitters especially in the case of the 1.3 GHz DCSO and the 2.856 GHz phase locked loop are a problem that has not been solved up to now. One point to consider experimentally is to increase the number of poles in the loop filters of the loops since the smaller proportional gain[37] can not supress the noise inside the loop bandwidth sufficently. An additional pole will also involve a new stability consideration of the loops. A smaller number of spurs in the locked loop phase noise in the 2.856 GHz module will also improve the integrated timing jitter of this module that will promisingly decrease to smaller than 100 fs. The phase noise measured at 27 MHz and 13.5 MHz shows also timing jitters higher than 100 fs. The theory to scale the phase noise by the division factor of N is not working here. The limitation can be found in the divider chips and the additional output amplifier in the divider modules used to generate these frequencies.
The investigation of harmonics shows that the modules meet the distance of harmonics to carrier.
The drift of the 1.3 GHz amplifier is in a tolerable range but the measurements have to be made for the 81 MHz amplifier as well.
The drift measurements of several RF sources has not been setup yet. The measurements include two complete low power parts (LPP) and two 1.3 GHz phase locked loops driven by one reference source (figure 10). In order to localize the main causes for drifts at the outputs a complete analytic description of the correlation of output voltages at all frequencies generated in the two oscillator systems is necessary.
New VCO's for the 81 MHz and 108 MHz phase locked loops with superior phase noise performance have been shipped to DESY with first measurement results showing integrated timing jitters from 10 Hz to 1 MHz smaller than 55 fs. The performance of the entire distribution system includes the links of signals to remote tappoints in the facility. The sum of drifts generated in the M.O., the power amplifiers, the locally installed PLL's and the cables will all contribute to drifts of the reference signals at distant tappoints. The measurement of drifts in a coaxial distribution system between distances up to 300 m at FLASH is a future research topic. The possibility to monitor drifts over this distance has been shown [11].

[36] phase noise at 9 MHz could not be measured with our instrument that works with a minimum input frequency of 10 MHz

[37] due to the high tuning sensitivity of the VCO's

Acknowledgements

I would like to thank Prof.Dr.-Ing. Schünemann for supervising this thesis and increasing my interests for research topics at microwave frequencies.

Big thanks go to my botany companions and colleagues Jost Müller, Matthias Hoffmann, Matthias Felber, Frank Eints, Jean Randhan, Frank Ludwig and all who join us from time to time.

I would also thank the retired PhD student Norbert Pchalek for the many interesting discussions about work, and many topics that go beyond that.

Harry Busse introduced me to the mystery of Tangerine Dream and he knows what I mean.
Thanks go especially to all people who shared my work on the Master Oscillator like Henning Weddig, Krzysztof Czuba, Bibiane Wendland and others involved with this project.

My last but not least thanks go to Stefan Simrock who supported and still supports me for finish my master studies and partly work on this project.

A Blockdiagrams

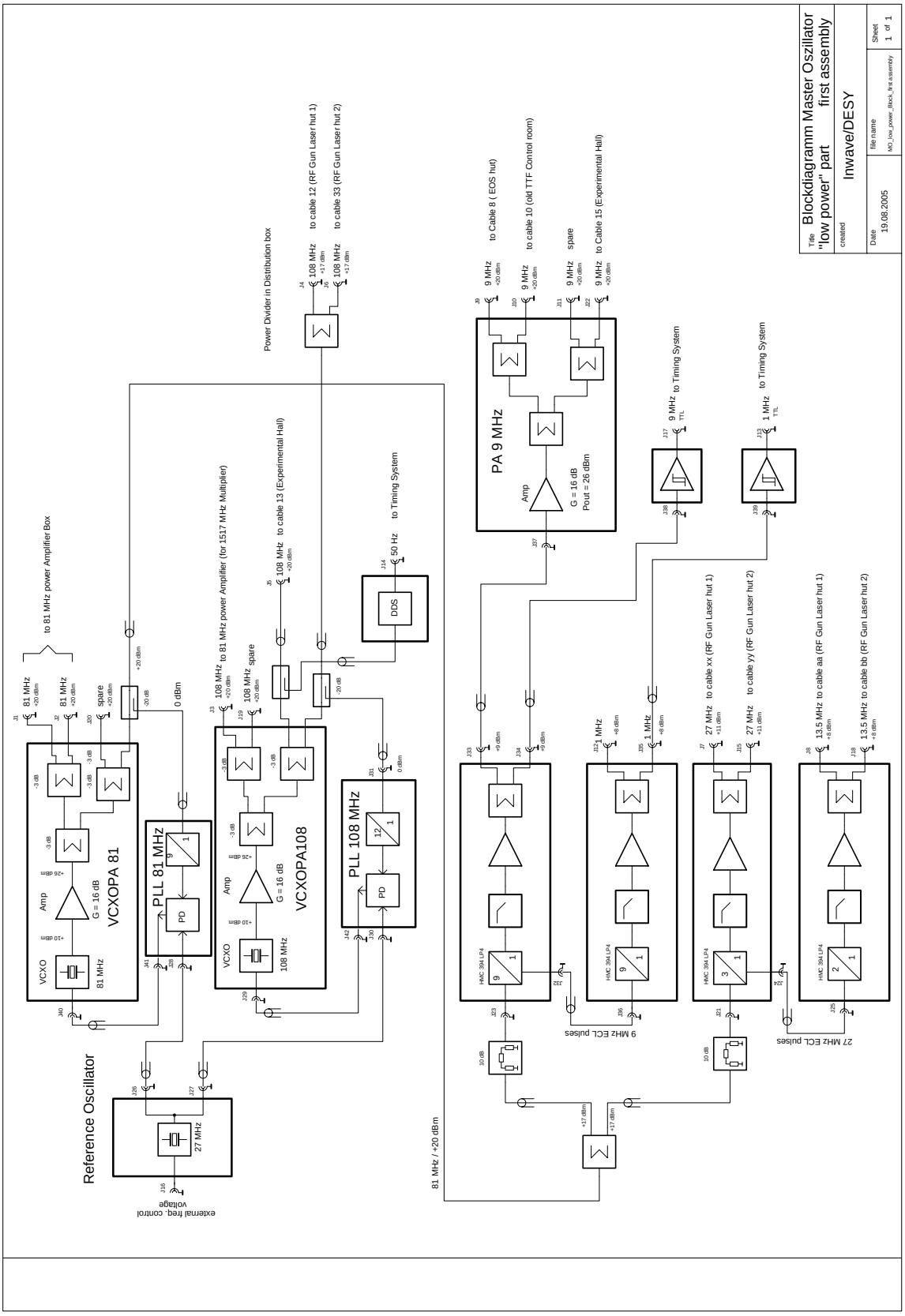

Figure 61: Blockdiagram low power part Master Oscillator

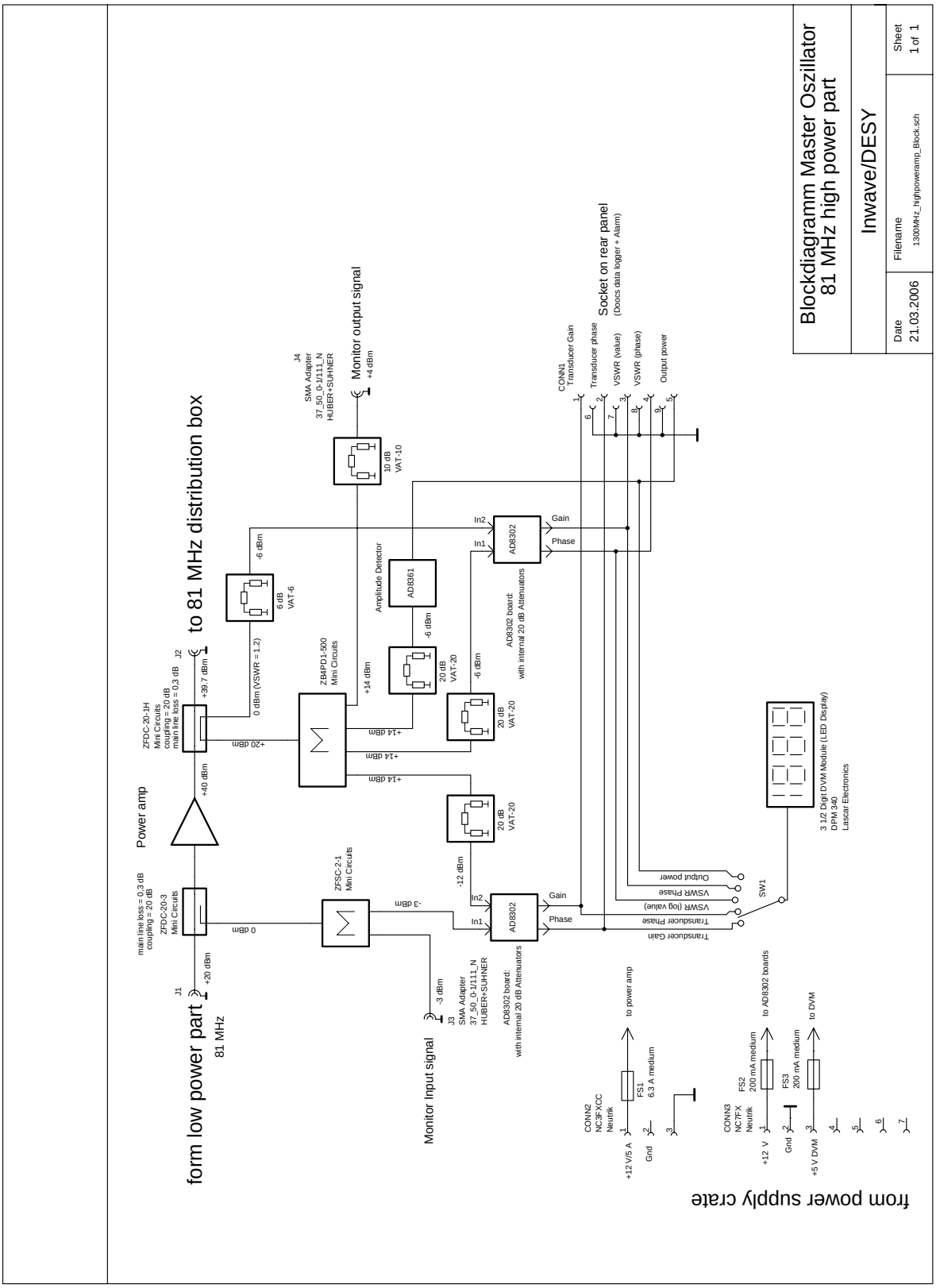

Figure 62: Blockdiagram of 81 MHz high power part Master Oscillator

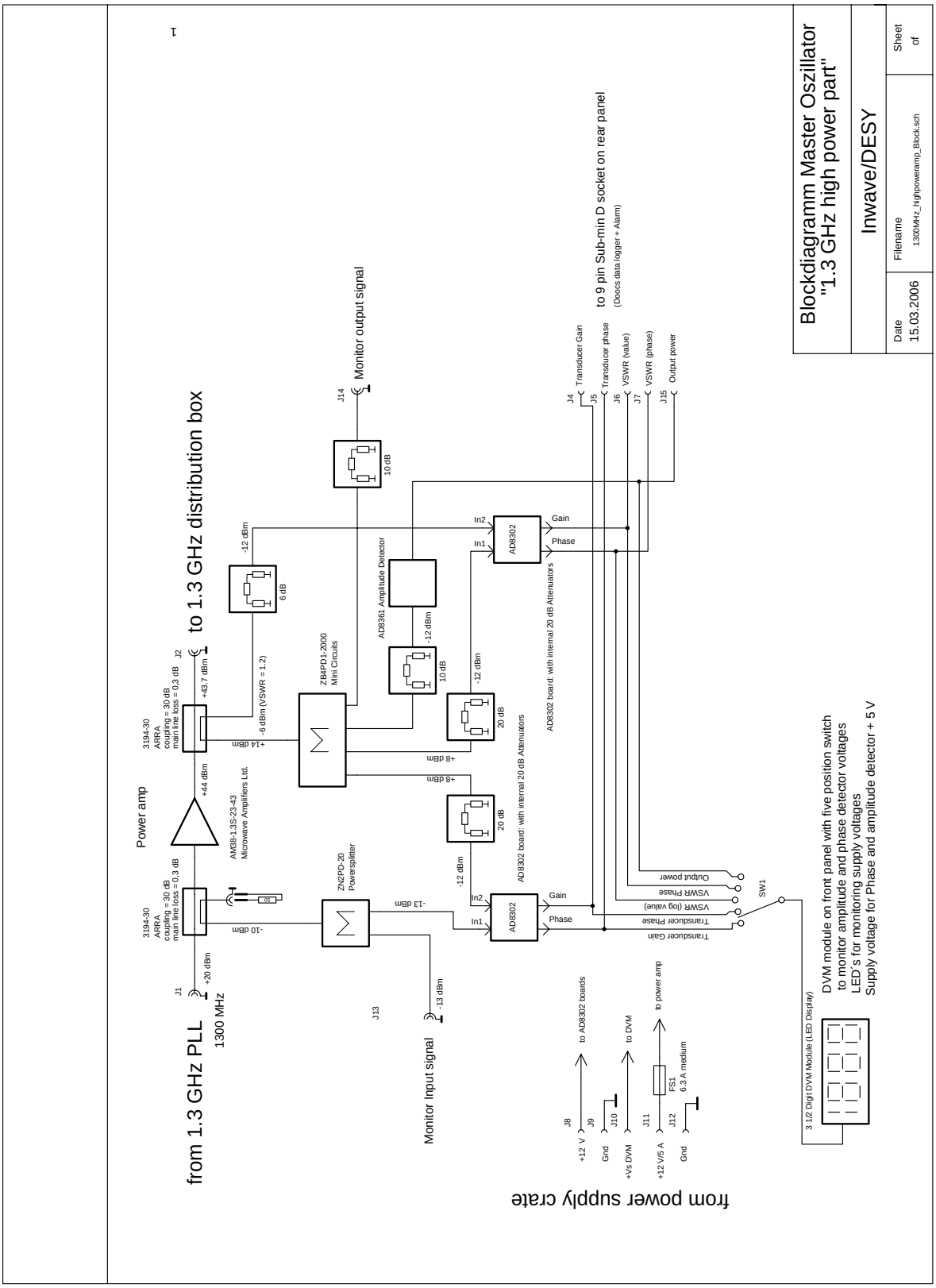

Figure 63: Blockdiagram of 1300 MHz high power part Master Oscillator

B Programming the ADF4153

For synchronizing the deflection cavity with the help of a fractional N divider synthesizer chip the registers in the chip have been programmed as follows.
Programming the Registers:
4 registers should be programmed [7]
Example: Bit pattern for synchronizing LOLA loading numbers:

reg0=reg0 (for decimal 0)
reg1=reg327681 (for bitpattern:1010000000000000001)
reg2=reg578 (for bitpattern:1001000010) or reg2=reg514 for inversed polarity of phasedetector with bitpattern : 1000000010
reg3=reg967 (for bitpattern:1111000111)
and the values for INT, FRAC and MOD should be entered like frac0...frac4095 [+ Enter].
Here:
frac612
mod1015
int140

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Confirmation

I confirm that i have written the thesis myself and only the references mentioned have been used.