ATCA-based LLRF System for XFEL

Demonstration at FLASH

Waldemar Koprek, DESY
for the XFEL LLRF team

Outline

- Introduction to ATCA
- LLRF System for the European XFEL
- Demonstration at FLASH
- Measurements

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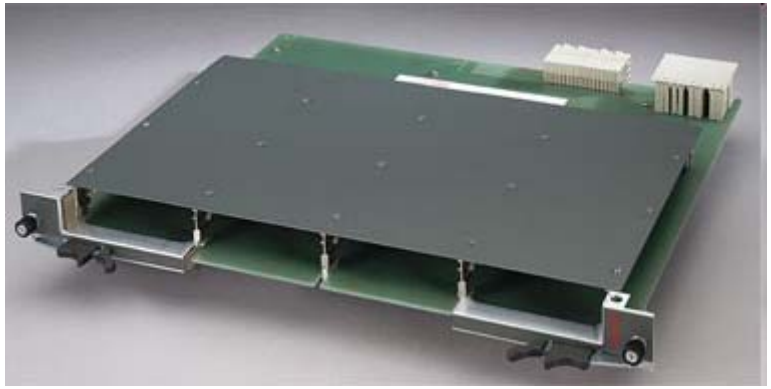
ATCA Standard

PICMG 3.0 – Advanced Telecommunications Computer Architecture

PICMG AMC.0 – Advanced Mezzanine Card



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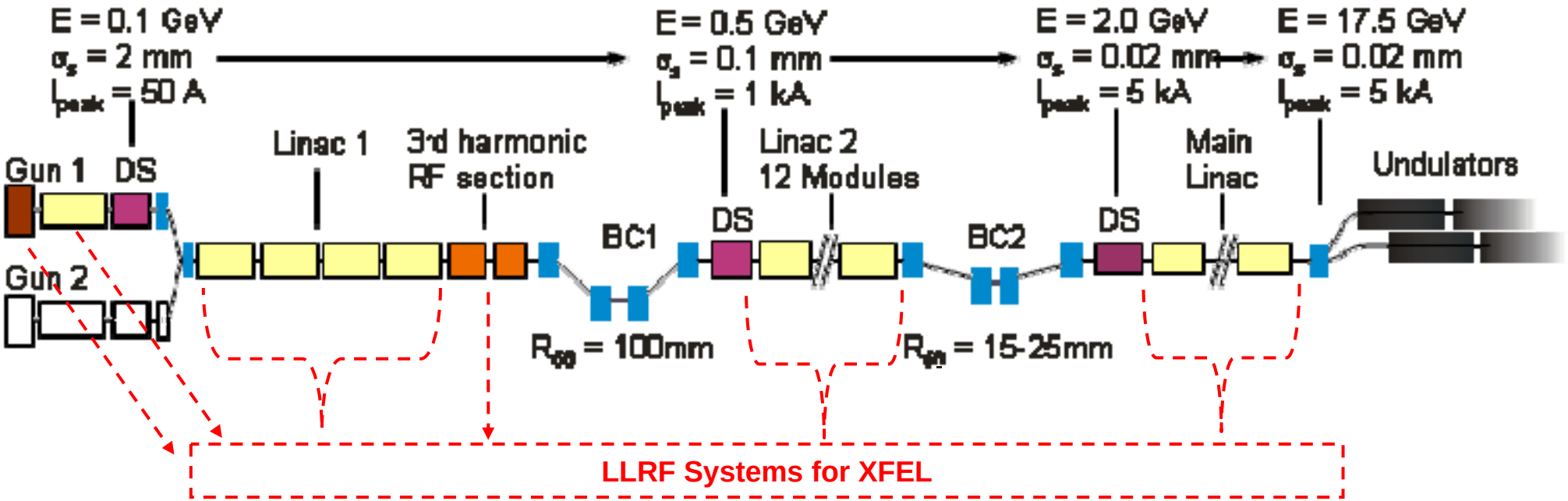
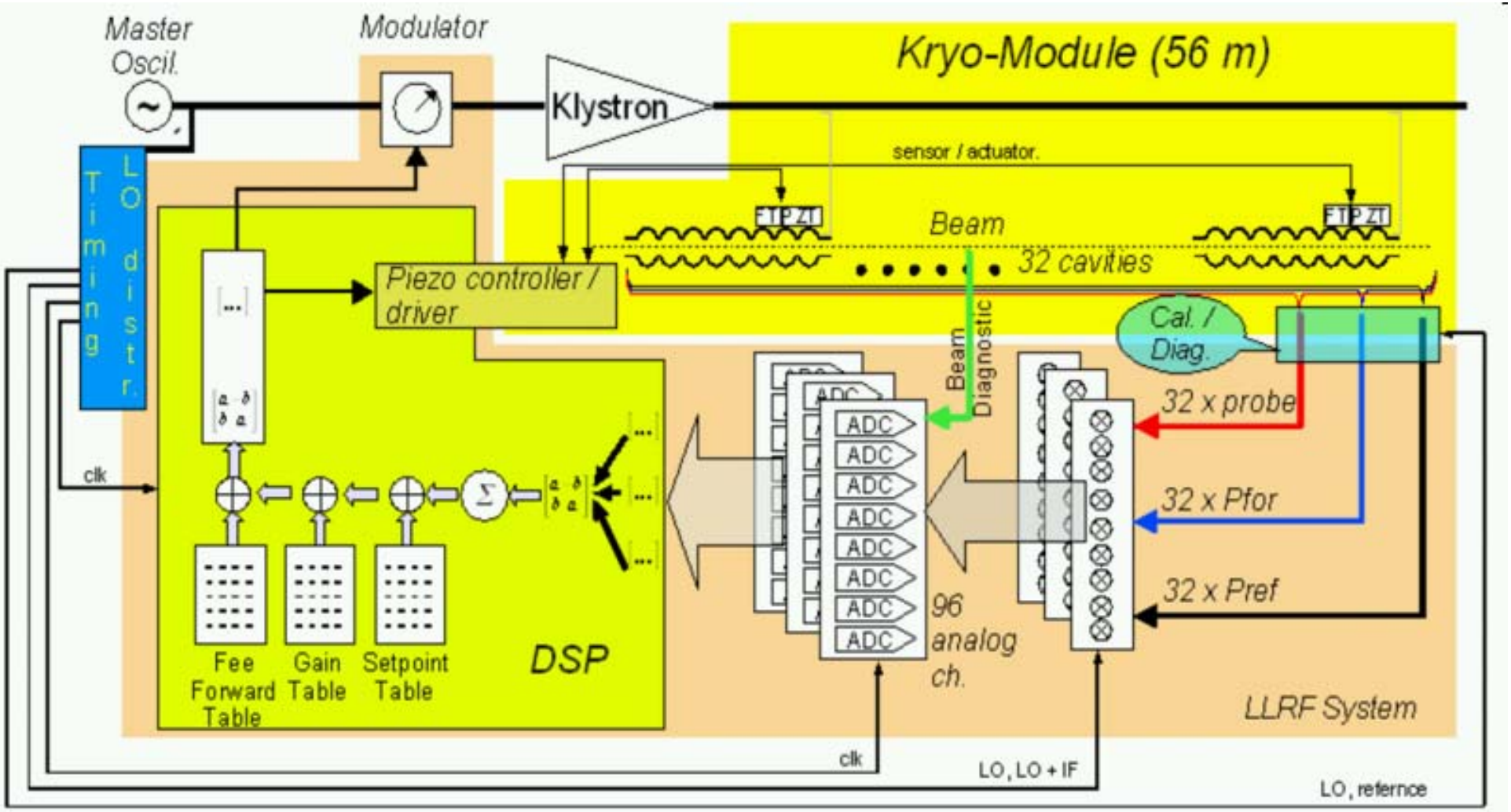
XFEL Overview



Architecture of the LLRF System for XFEL



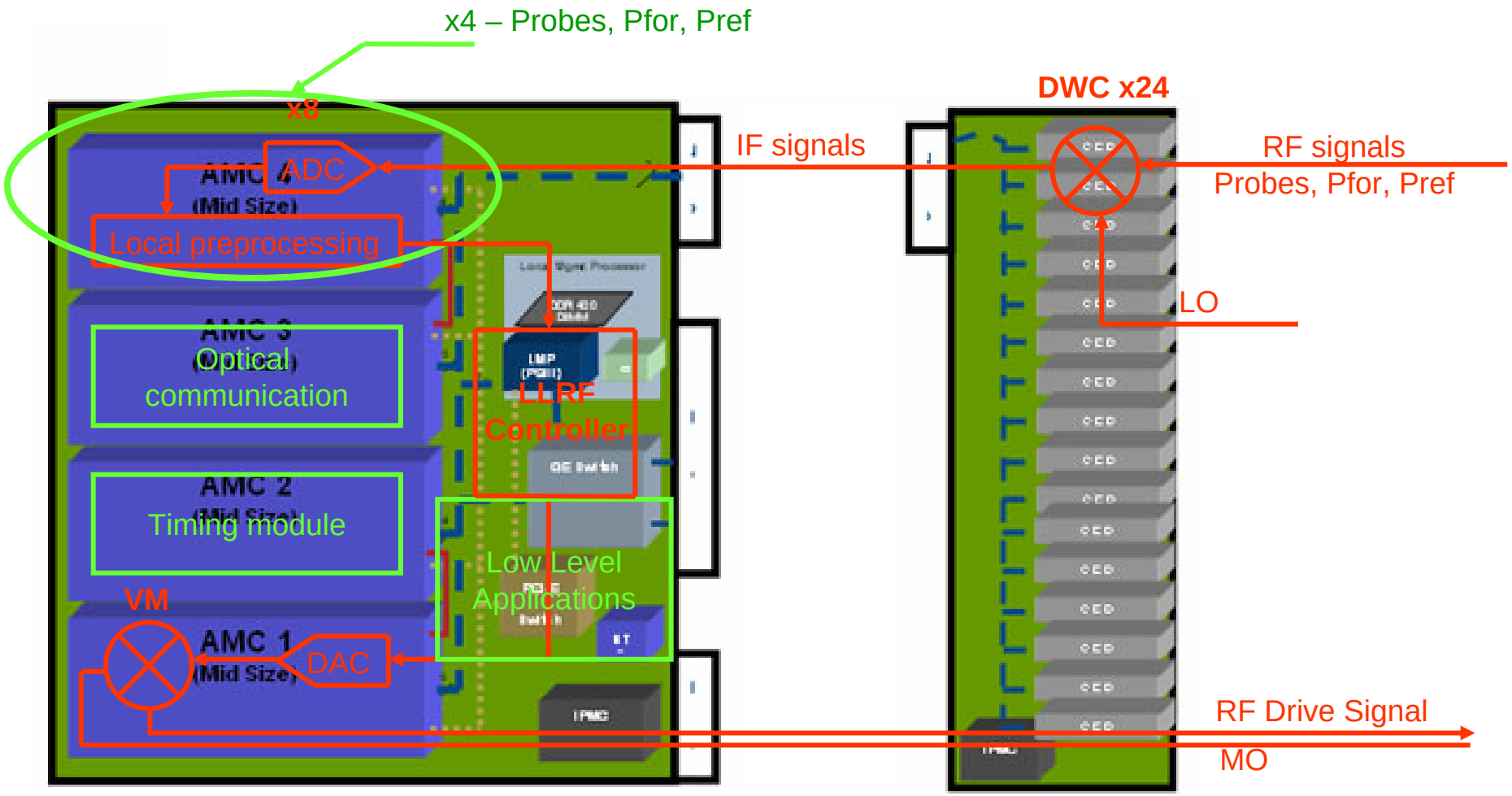
Decision for ATCA

- Future LLRF systems will require simultaneous data acquisition of up to 100 fast ADC channels at sampling rates of around 100 MHz and real time signal processing within a few hundred nanoseconds.

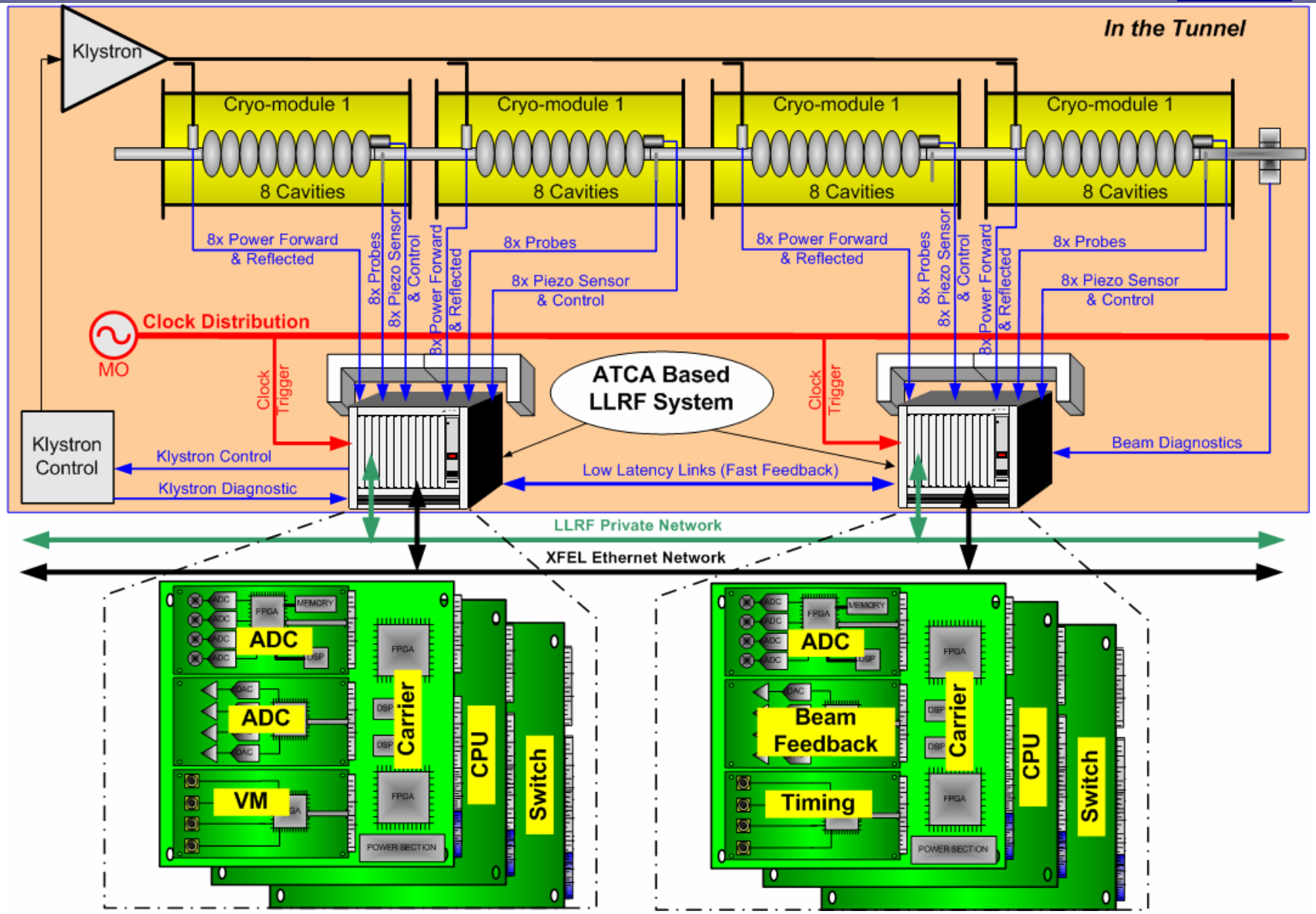
- Also desirable are modularity and scalability of the design as well as compatibility with accelerator instrumentation needs including the control system.

- All these requirements can be fulfilled with the new telecommunication standard ATCA

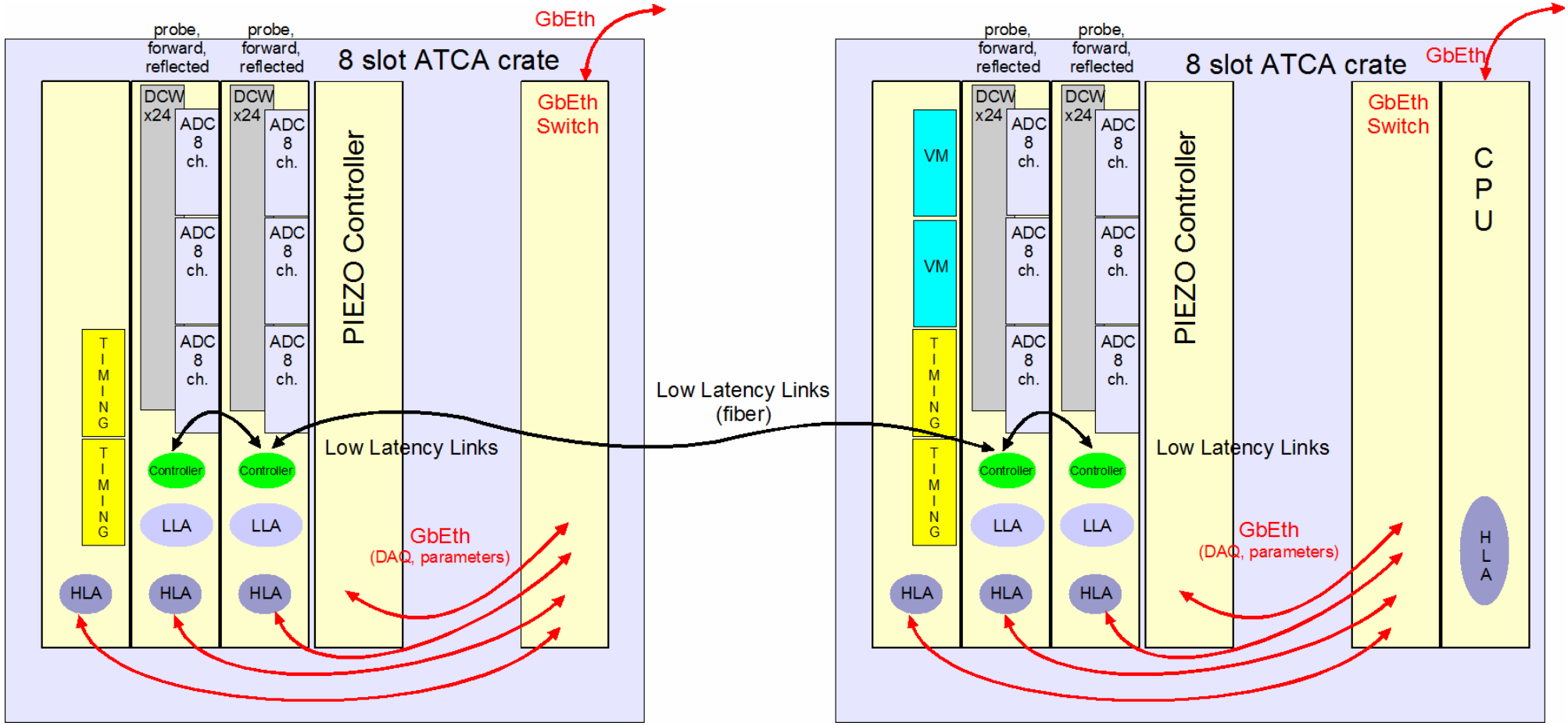
Architecture of LLRF System



Hardware Design



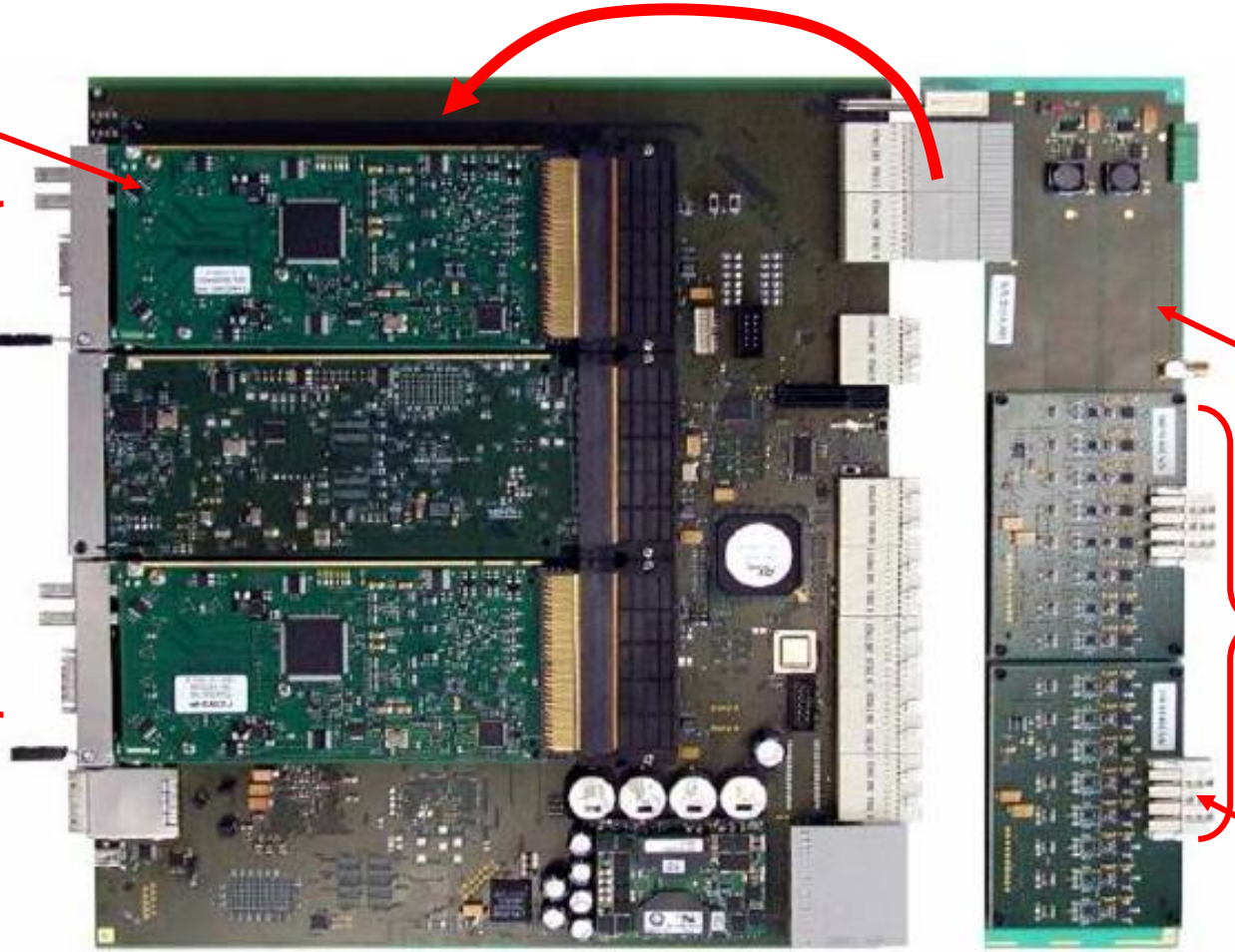
Configuration of LLRF in ATCA Crate



ATCA Carrier with AMC slots and RTM

Stacked 1-wide AMC ADC's & IO AMC's, connectors

105 MHz 14 bit 8 Ch COTS ADC's



RTM

Down-converters To 25 MHz IF

1.3 GHz RF Inputs

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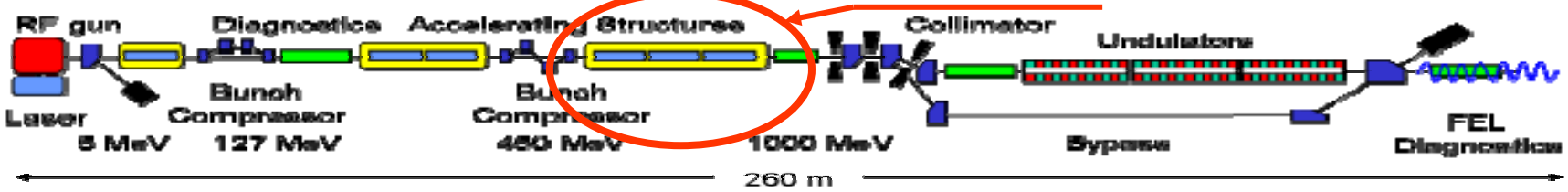
Demonstration Goals

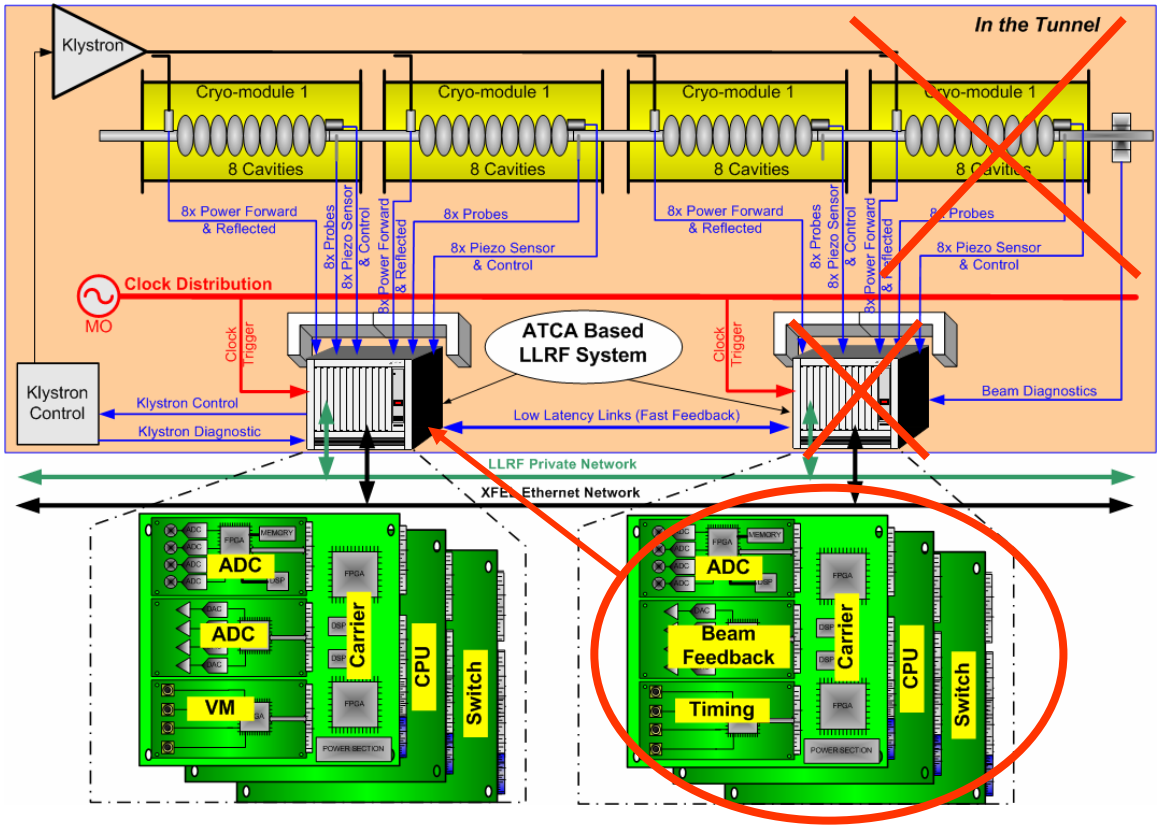
Demonstrate that ATCA is the right standard for LLRF system at XFEL

Objective	**Comment**
Analog IO	Demonstrate the noise added from entrance to rear transition module through Zone 3 and carrier to AMC module is not degraded
Communication links	Demonstrate that the scheme of Low Latency Links, PCIe and GbE is functional.
Operation in accelerator environment	Demonstrate that the ATCA based LLRF is functional in the noisy accelerator environment.
Rear transition module	Demonstrate the concept of rear transition modules with downconverters
Timing distribution	Demonstrate timing distribution functionality
Timing jitter	Demonstrate that the measured timing jitter is adequate for LLRF control.
IPMI	Demonstrate the IPMI implementation.

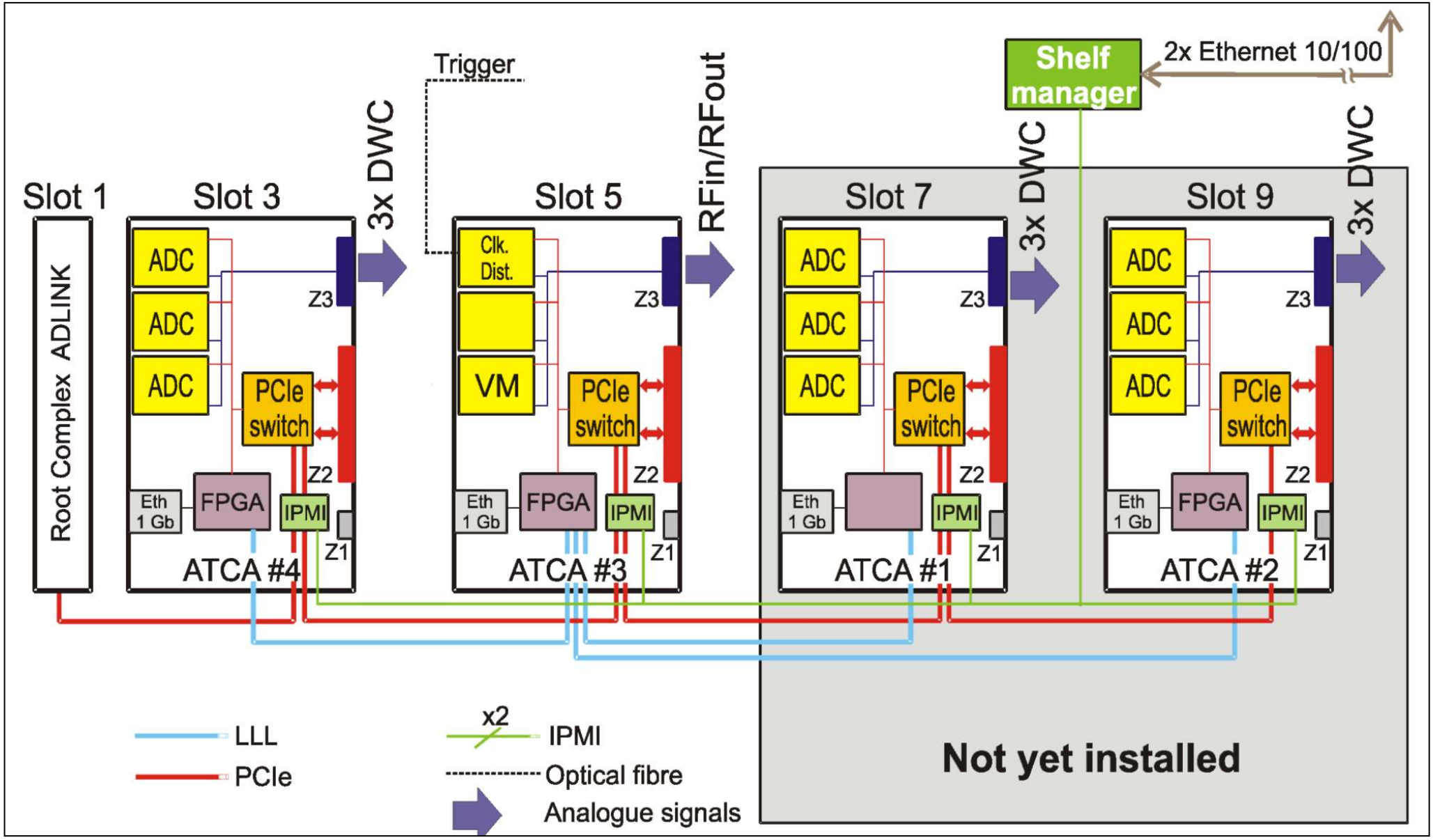
ACC4/5/6 at FLASH

ACC4/5/6 = 24 cavities

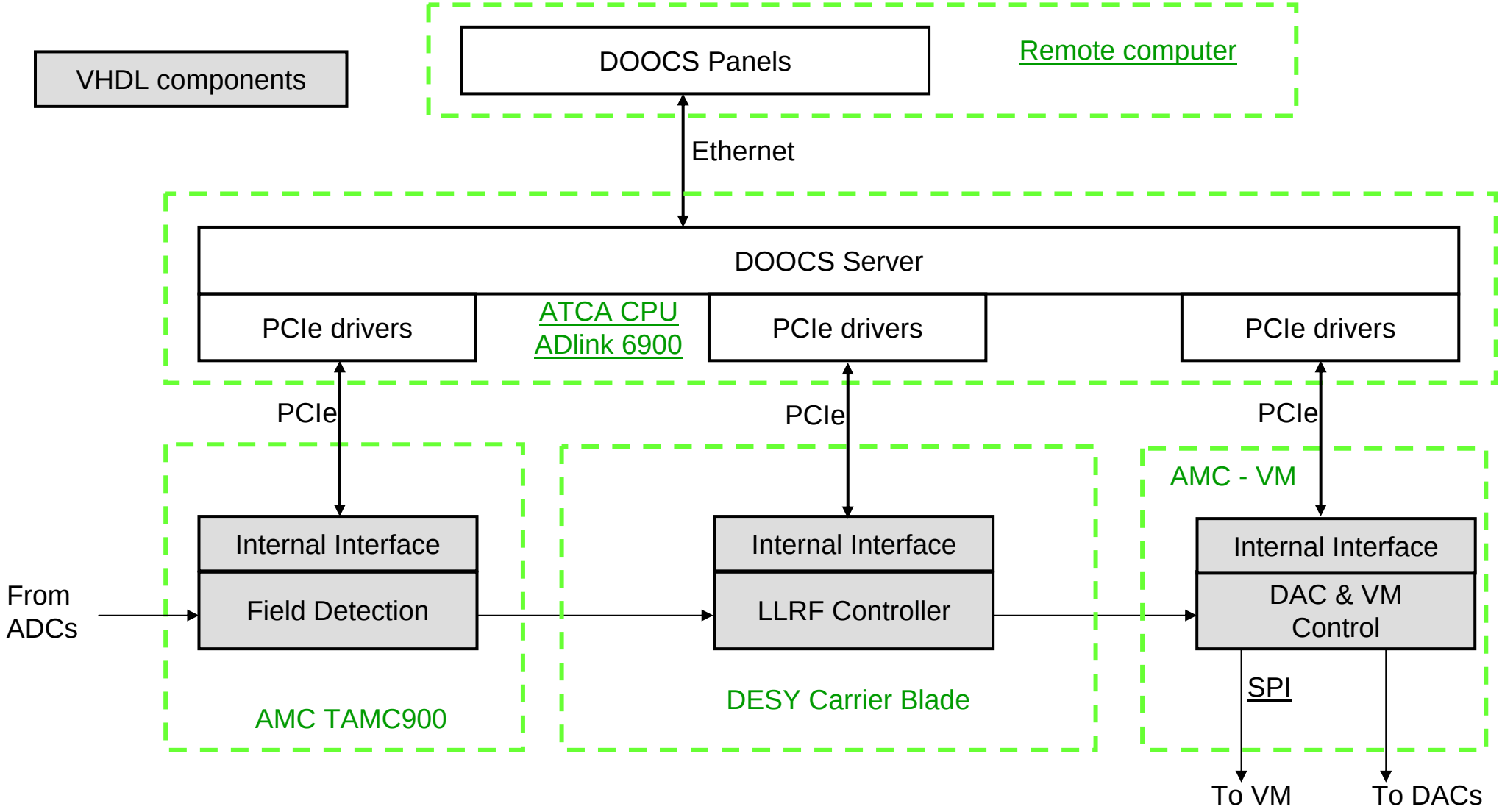




ATCA Configuration at FLASH

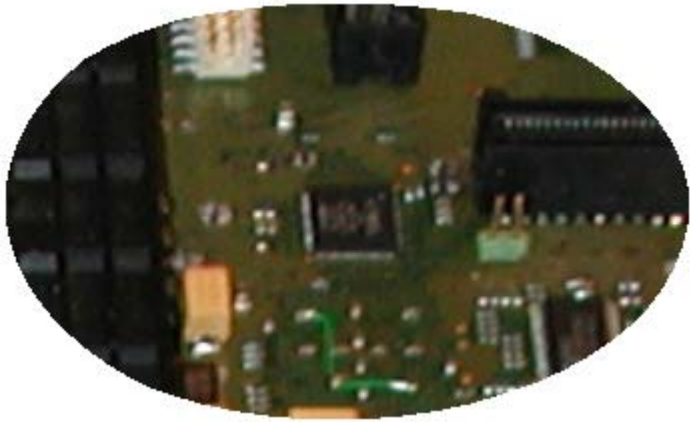


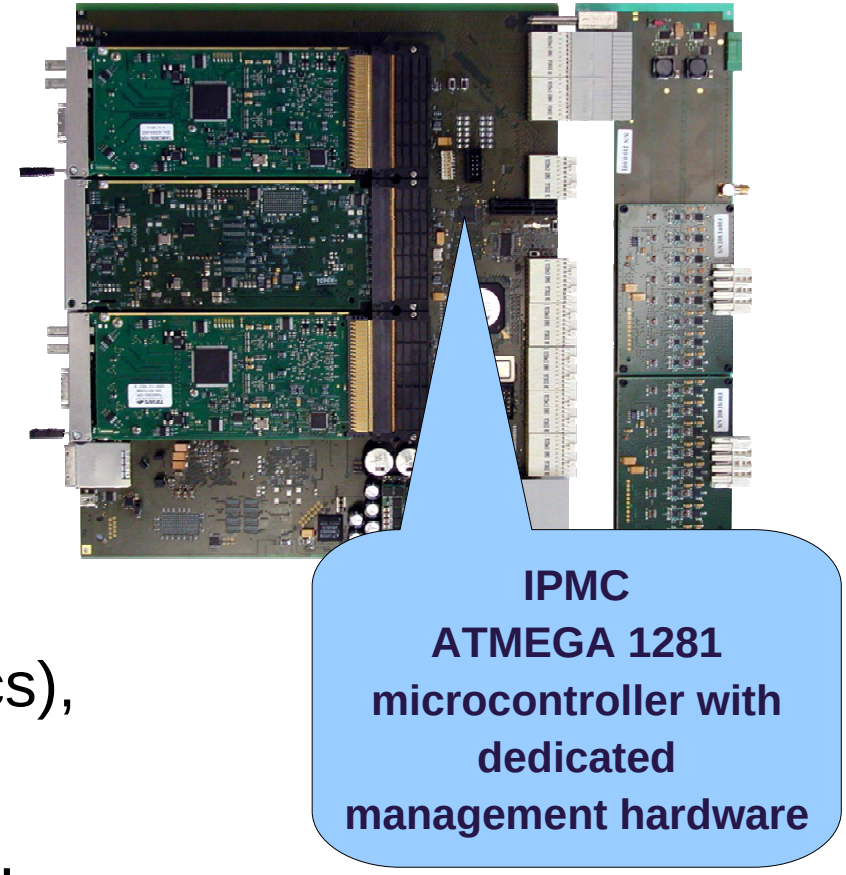
Software Architecture



TP26, Wojciech Jalmuzna – "Development of Functional Modules for LLRF Field Controller"

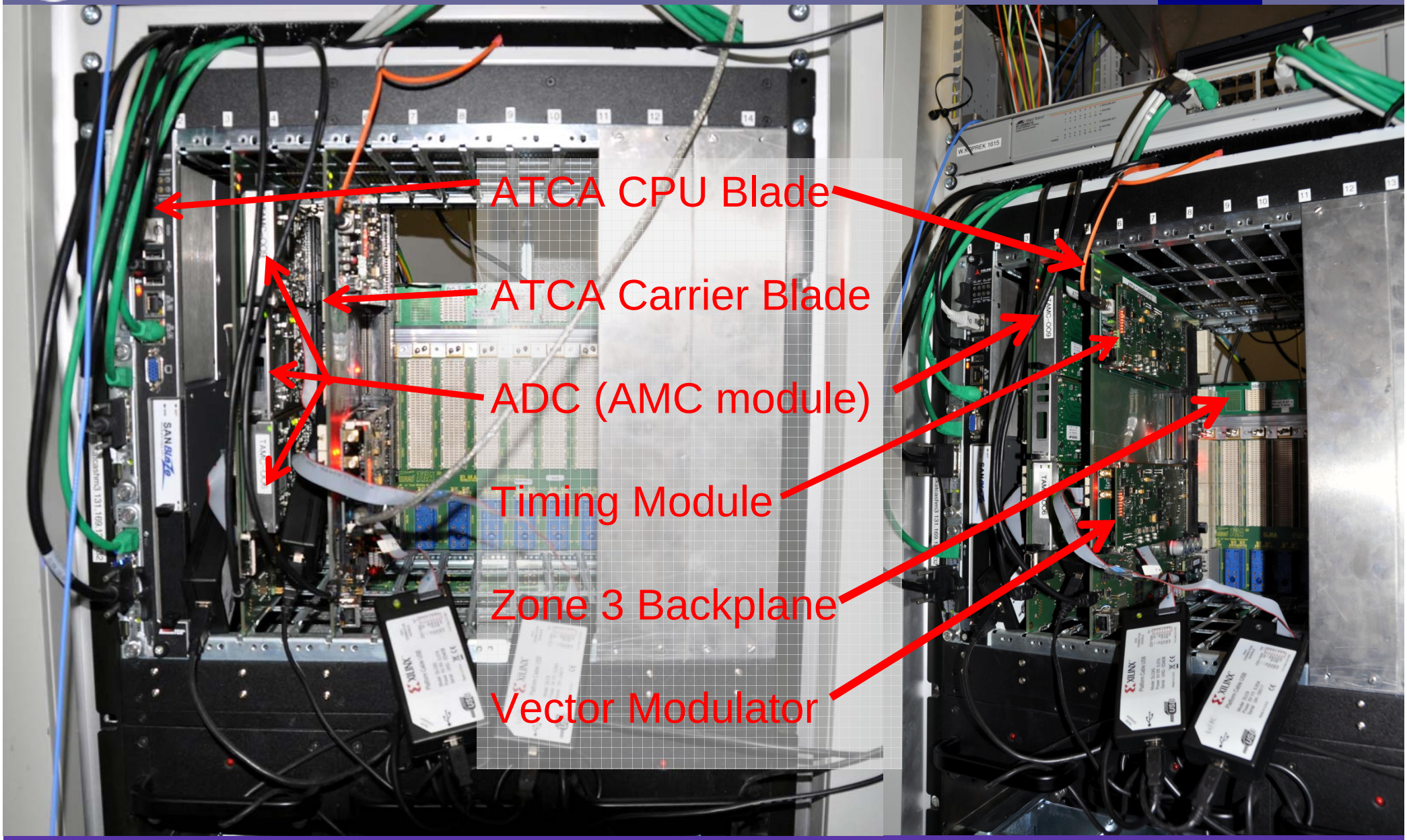
Intelligent Platform Management Interface (IPMI)



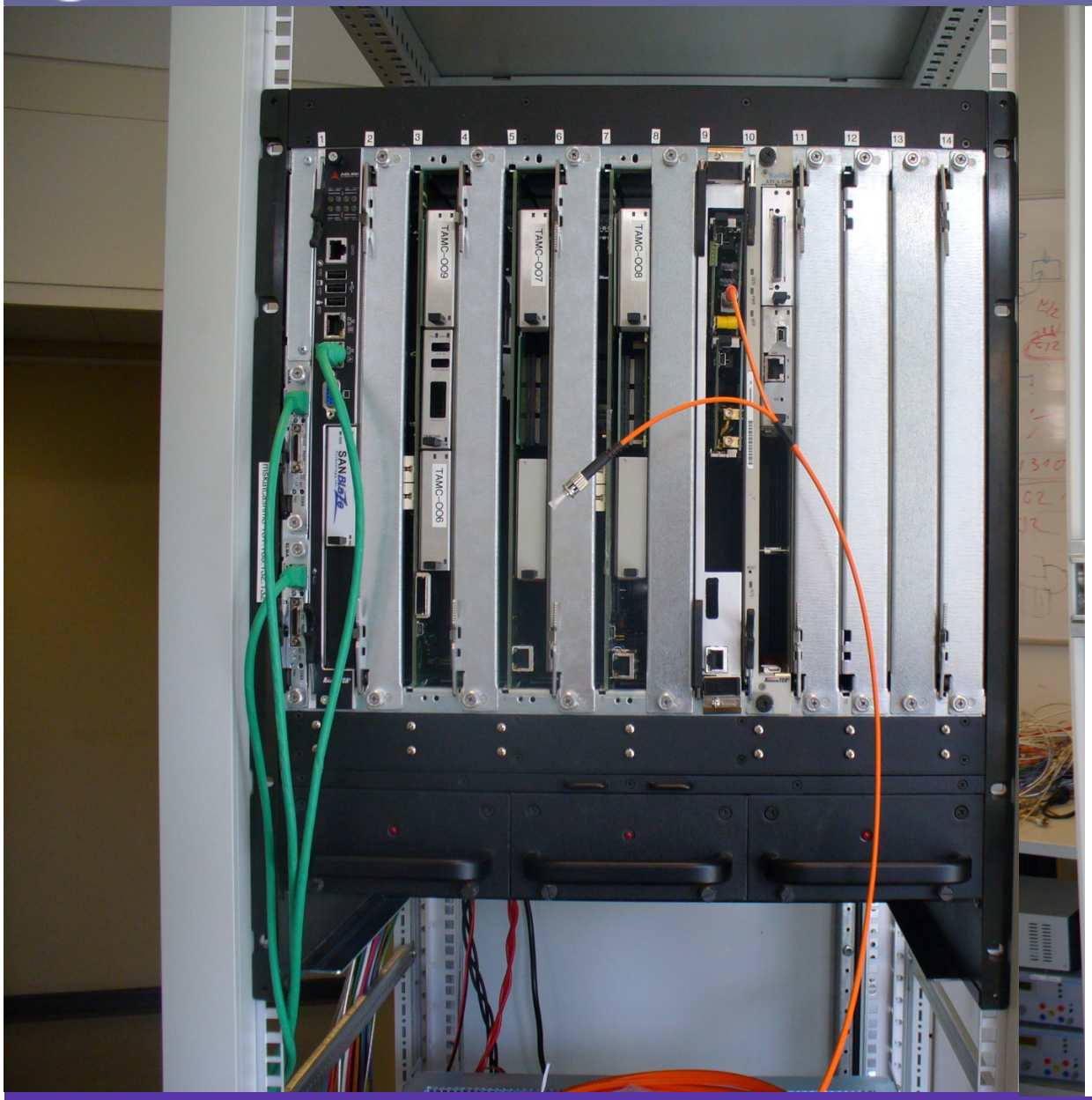


- Management of ATCA carrier blades,
- Management of AMC modules,
- Monitoring of ATCA health (diagnostics),
- E-Keying for PCIe, Gb Ethernet and user defined Low Latency Connection,
- Monitoring of temperature, power supply, clocks, etc...

Set-up at FLASH with 2 carrier boards



Set-up in Lab with 4 Carrier Blades

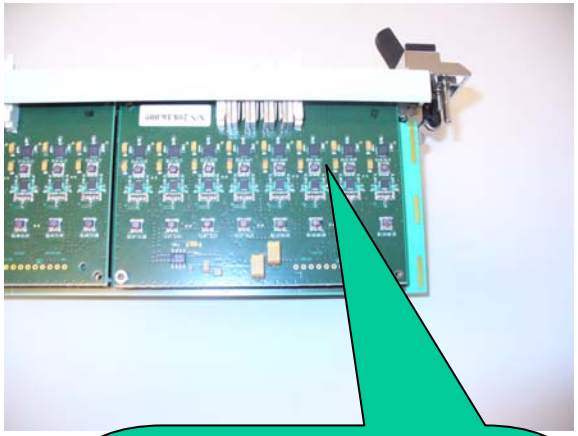


COTS

TEWS TAMC900

RTM Module
from Cryoelectra

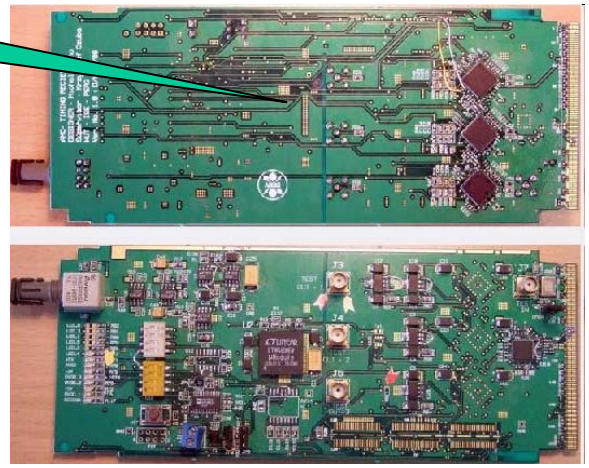
ADlink CPU 6900

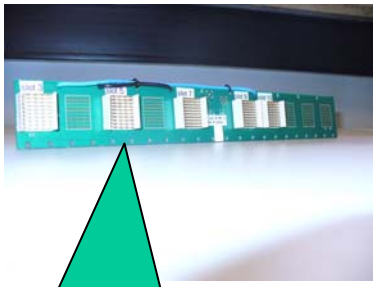


Downconverter
from Cryoelectra

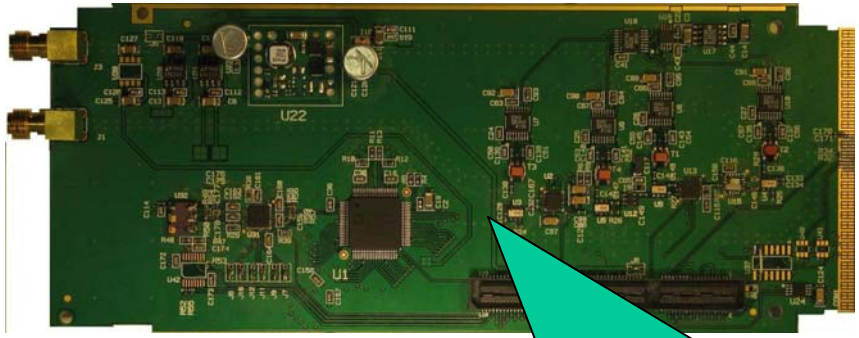
In-house development

AMC-TIM – Timing Module

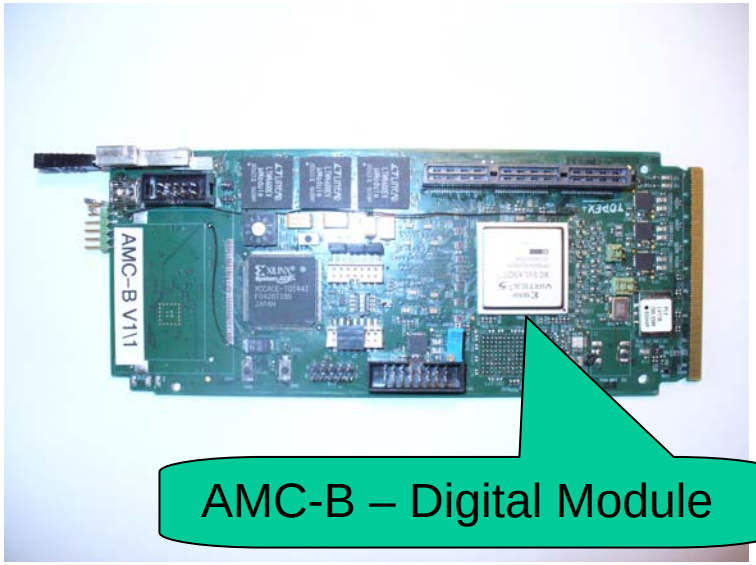




Zone 3 Backplane

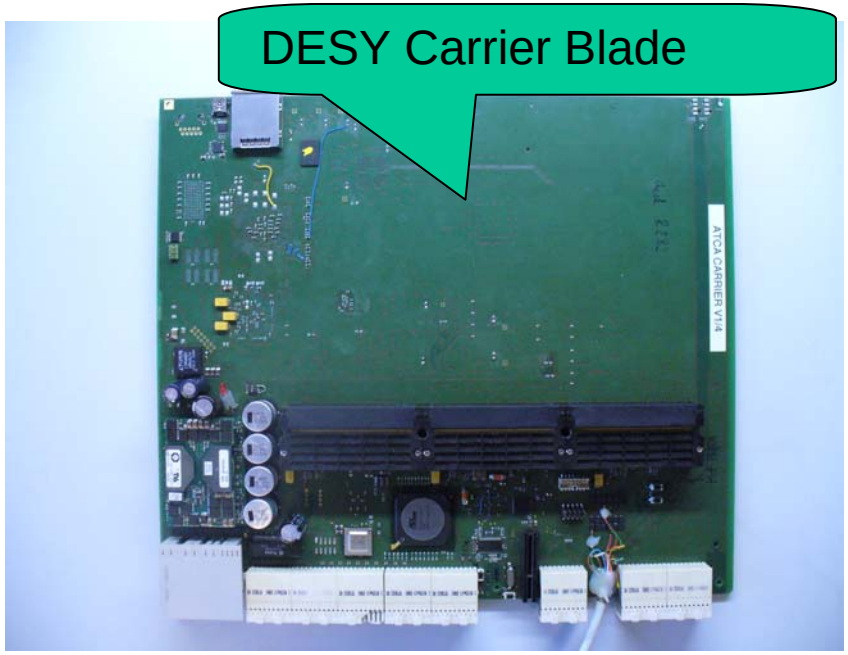


AMC-VM – Vector Modulator

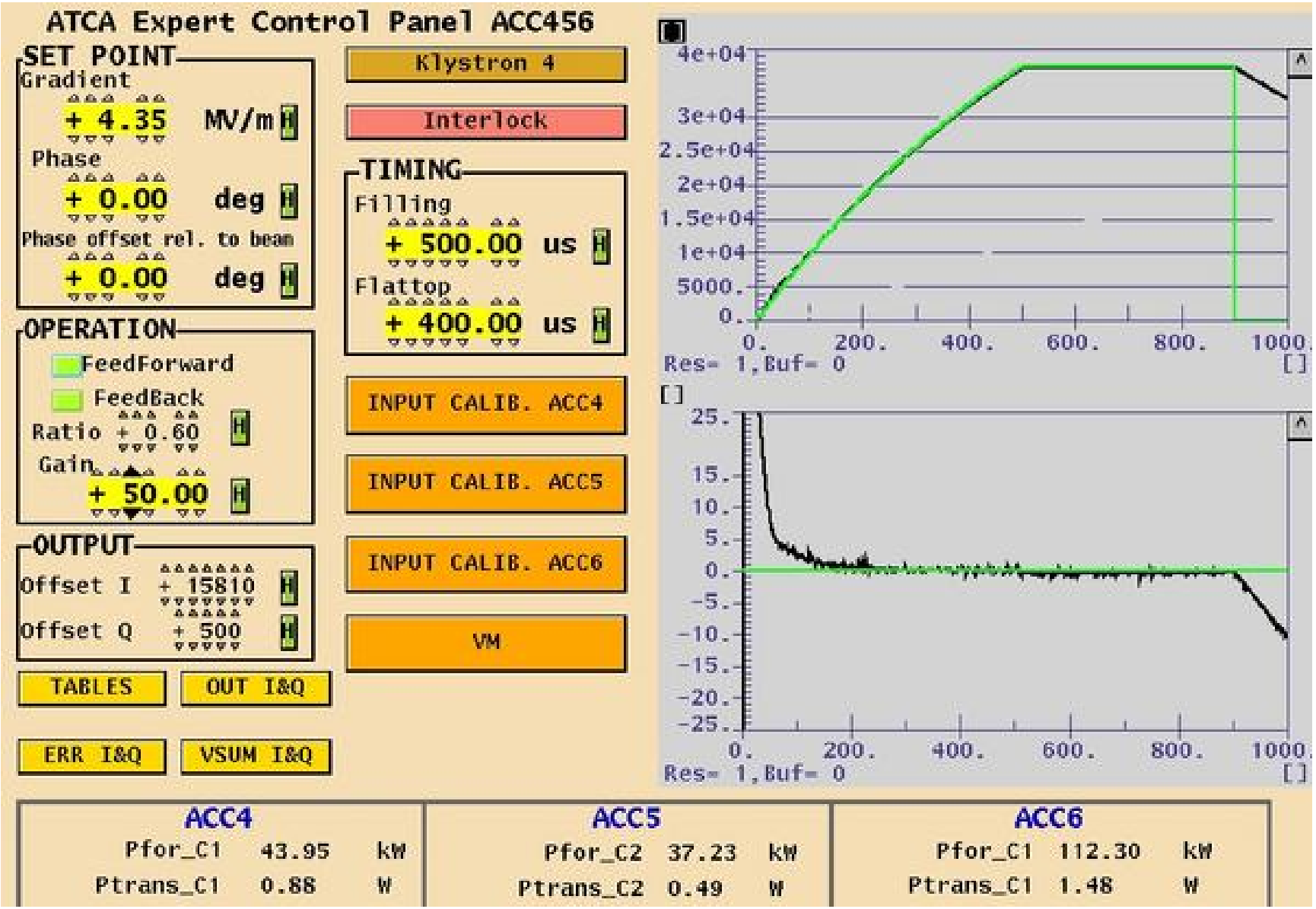


AMC-B – Digital Module

DESY Carrier Blade



Operator Interface



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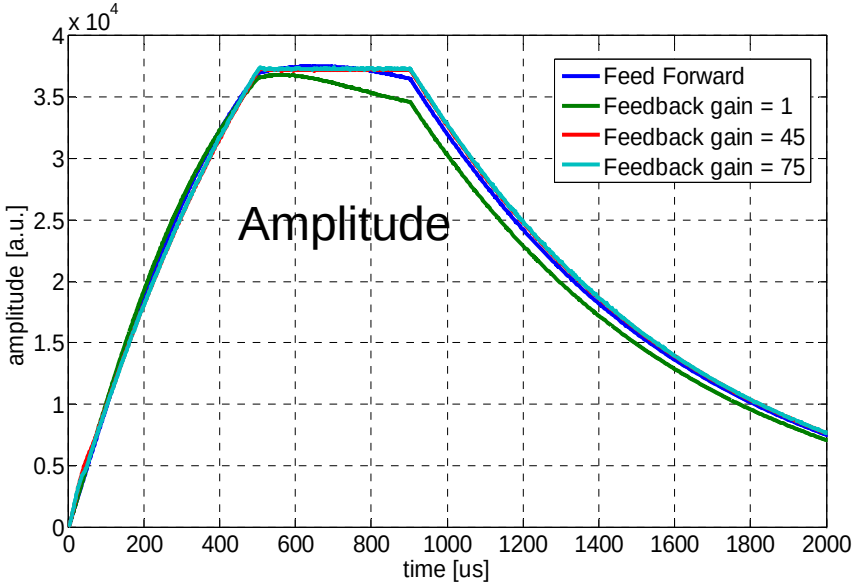
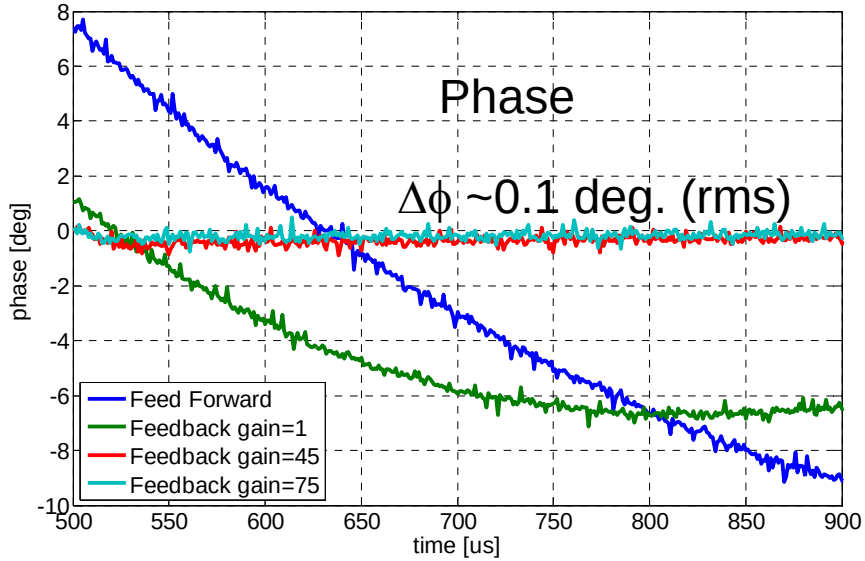
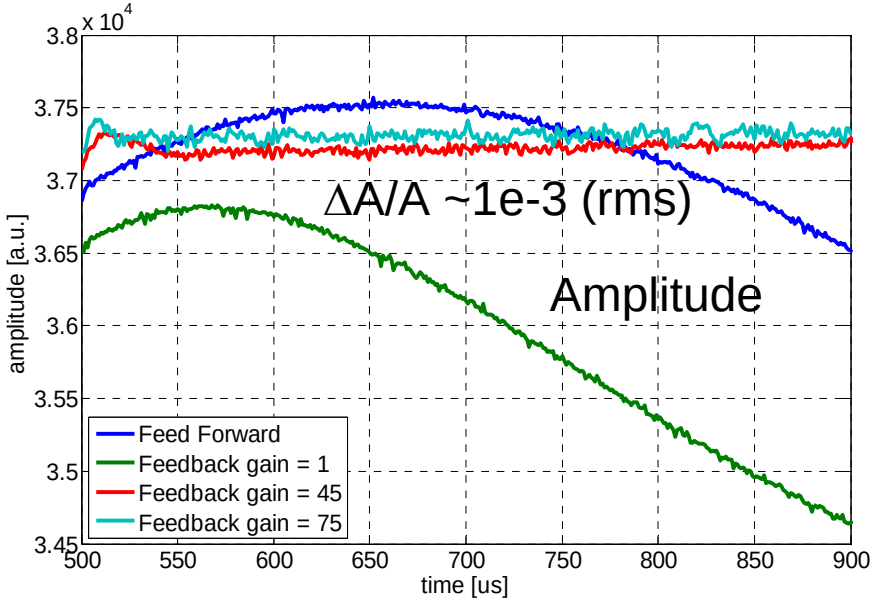
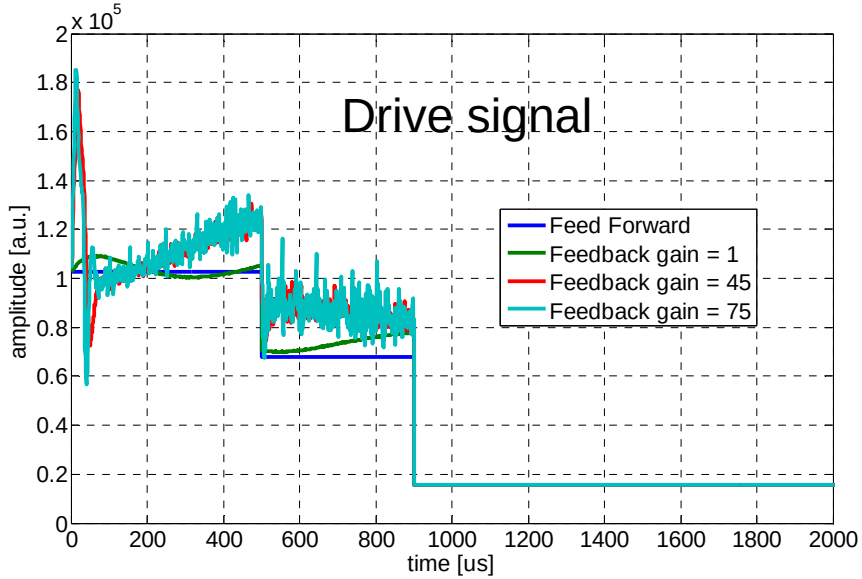
Amplitude and Phase Control







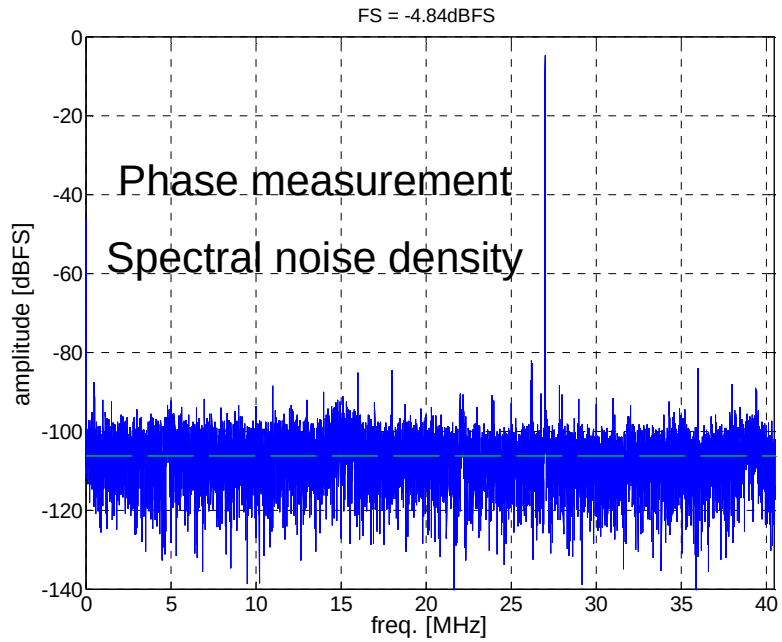


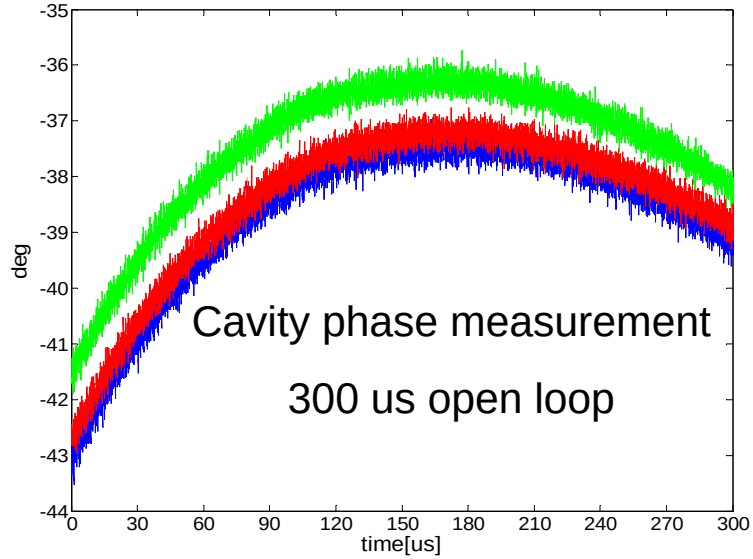
Crosstalk, Noise and Timing Jitter

Preliminary Performance Data

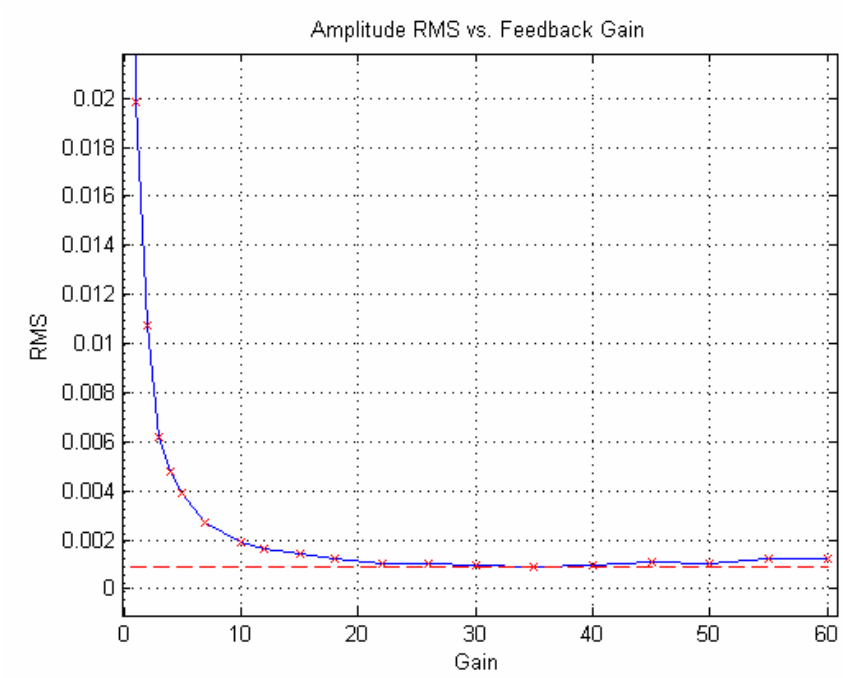
- Channel isolation >80 dB @50MHz
  (presently limited by downconverter)
- Noise < 200 μV (rms)
  consistent with 14-bit ADC, 200 MHz bandwidth
- Timing jitter < 15 ps (rms) @ 81 MHz
  (upper limit, could be dominated by RF

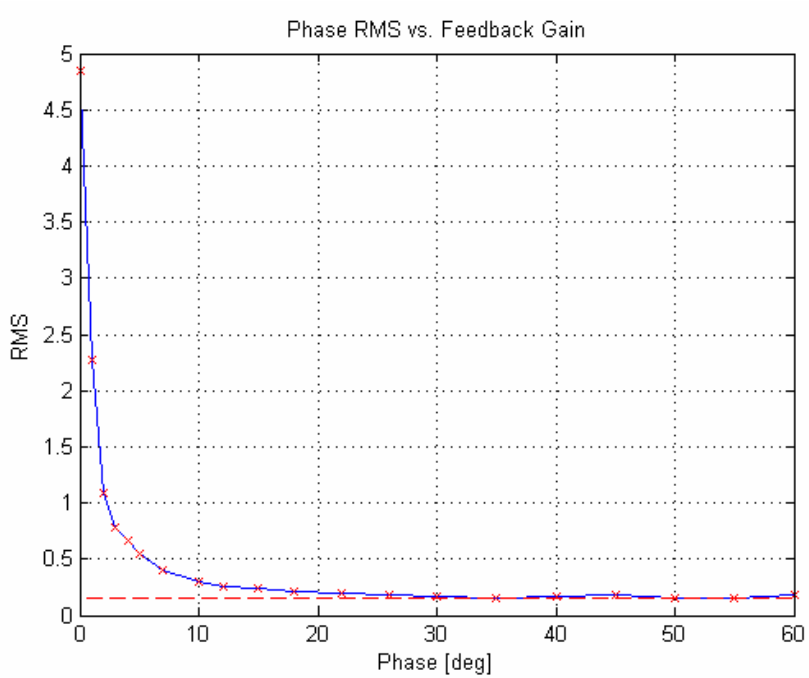
	ADC1	ADC2	ADC3	ADC4	ADC5	ADC6	ADC7	ADC8
ADC1 on	-67.87	-48.14	-66.86	-66.39	-73.71	-69.90	-67.11	-71.38
ADC2 on	-48.35	-67.79	-68.14	-74.08	-69.35	-71.00	-67.86	-72.67
ADC3 on	-59.51	-66.47	-68.09	-52.43	-66.08	-70.39	-66.98	-72.60
ADC4 on	-65.52	-69.55	-49.03	-68.03	-68.82	-69.81	-66.69	-70.78
ADC5 on	-73.27	-73.27	-67.81	-69.82	-66.44	-44.35	-63.30	-69.77
ADC6 on	-2.92	-0.45	0.56	-3.24	17.30	-8.12	4.08	8.28
ADC7 on	-76.22	-70.18	-69.39	-77.31	-65.34	-70.27	-68.47	-45.76
ADC8 on	-70.80	-63.62	-62.15	-69.65	-67.48	-62.79	-52.15	-64.50





Gain Scan





Min = 0.945e-3

for feedback gain = 35

Min = 0.98 deg

for feedback gain = 35

Conclusion

- The demonstration of the ATCA-based LLRF system at the FLASH user facility has verified that this standard can be employed for physics applications.

- Although standard is quite new commercial components and even complete systems are already available for physics applications.
  - Several physics labs are already using or evaluating the ATCA and μTCA standard

- First tests of the ATCA-based LLRF system show that it can be used for main linac at XFEL

Plans

- Final design of the ATCA-based LLRF system for XFEL
  - better design of downconverter
  - modification of the timing distribution concept in the ATCA shelf
  - replacement of PCIe links by 1Gb Ethernet
- Installation of ATCA development systems at FLASH during shutdown
  - at least one system at ACC45

Project Participants

- **Technical University of Lodz, DMCS, Poland**
  - Wojciech Cichalewski
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  - Dariusz Makowski
  - Adam Piotrowski
  - Sergiusz Szachowalow
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  - Samer Bou Habib
  - Lukasz Butkowski
- **The Andrzej Soltan Institute for Nuclear Studies, Swierk, Poland**
  - Jaroslaw Szewinski
- **DESY, Hamburg, Germany**
  - Mariusz Grecki
  - Tomasz Jezynski
  - Maciej Kudla
  - Frank Ludwig
  - Stefan Simrock
  - Henning Weddig