Cavity Detuning Computation and Its Implementation in FPGA

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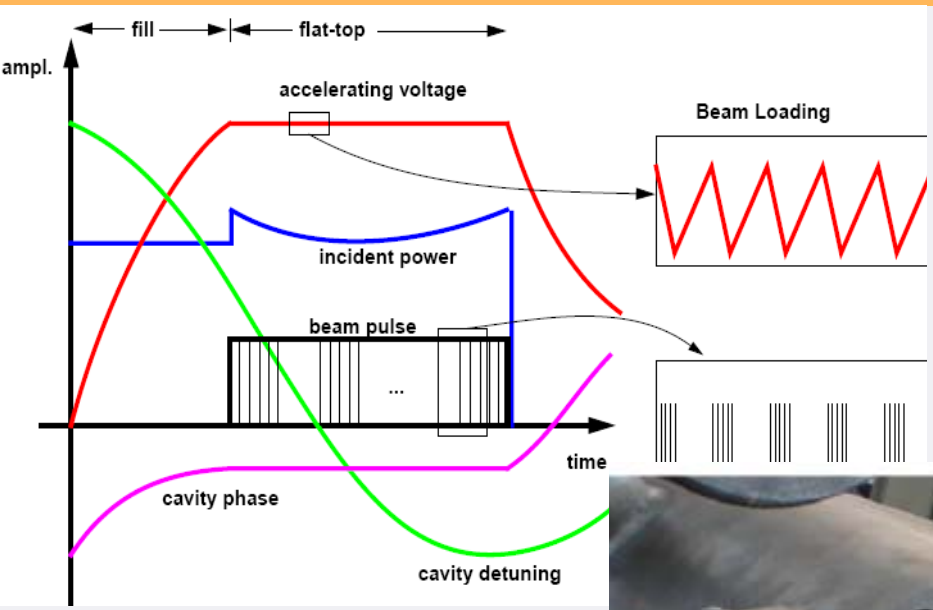
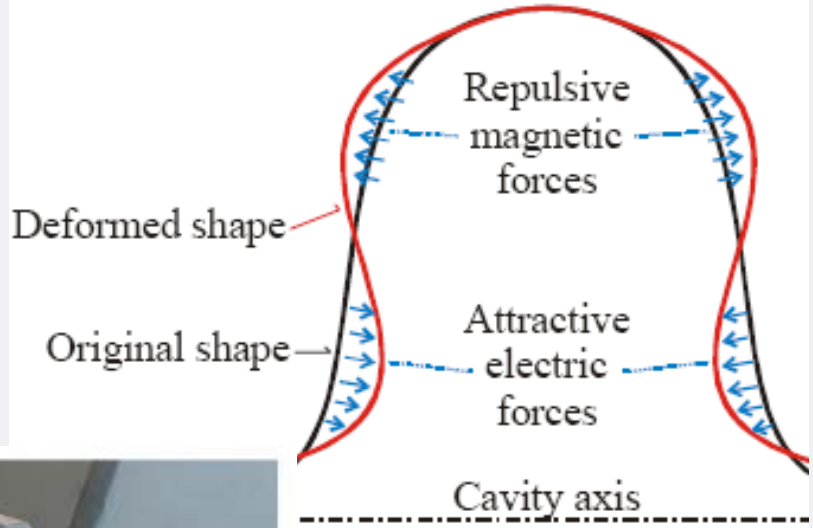
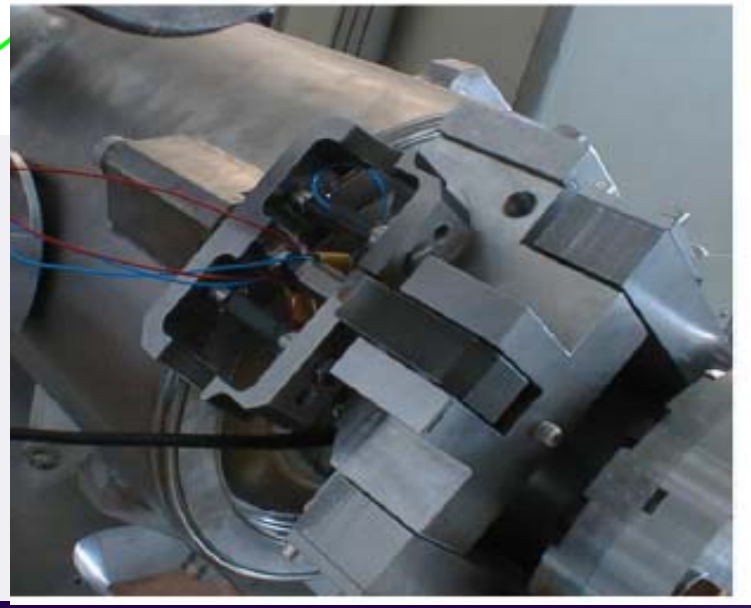
Agenda

- Motivation
- Block diagram of detuning computation
- Implementation structure
- Block diagram of various blocks
- FPGA resource usage
- Detuning Tool Tests (ACC1, MTS, ACC6)
- Conclusions and future plans

Motivation


fill
flat-top
ampl.
accelerating voltage
Beam Loading
incident power
beam pulse
...
time
cavity phase
cavity detuning

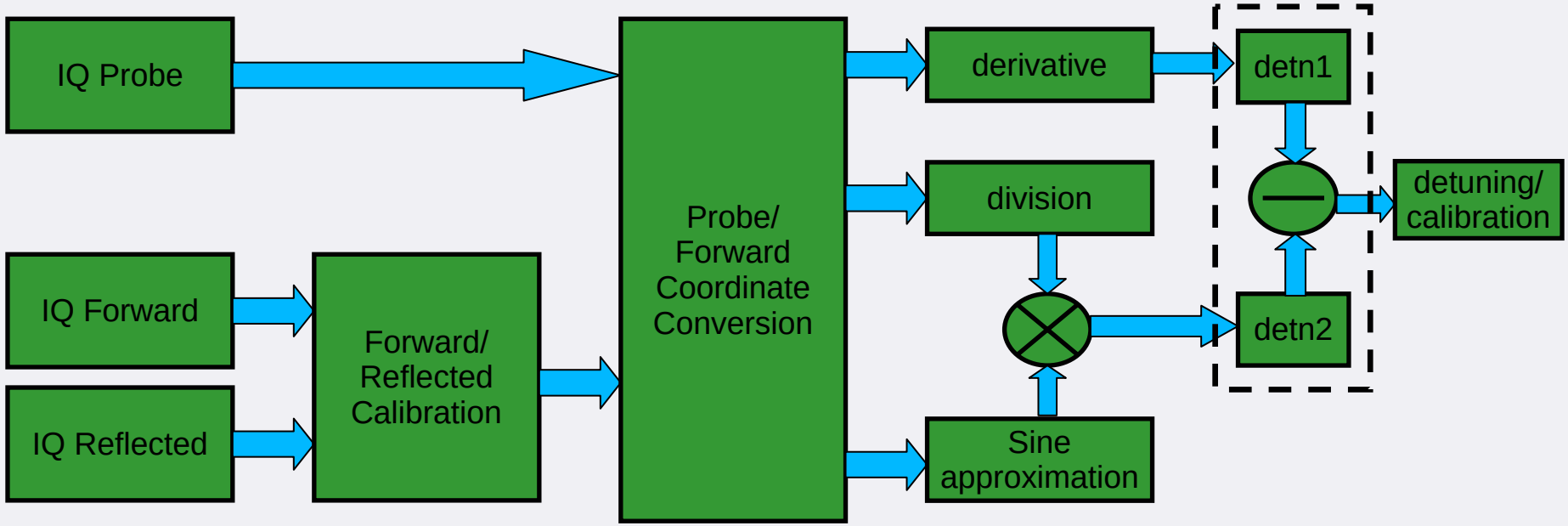

Repulsive
magnetic
forces
Deformed shape
Original shape
Attractive
electric
forces
Cavity axis



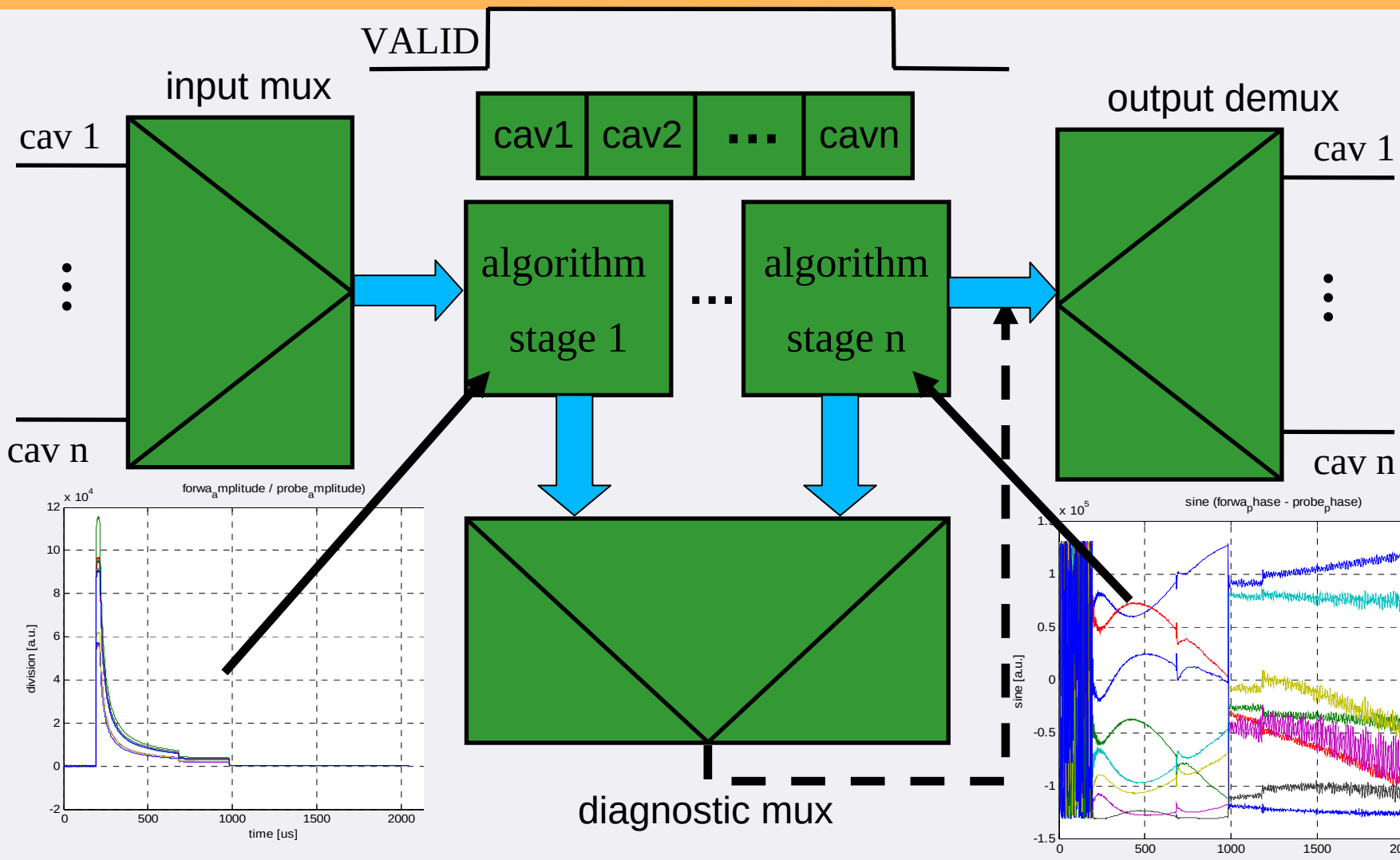
Block Diagram of Detuning Computation

$$\Delta\omega = -\frac{1}{2\cdot\pi}\left(\frac{d\phi_{probe}}{dt} - 2\cdot\omega_{1/2}\cdot\frac{|U_{forward}|}{|U_{probe}|}\cdot\sin\left(\phi_{forward}-\phi_{probe}\right)\right)$$

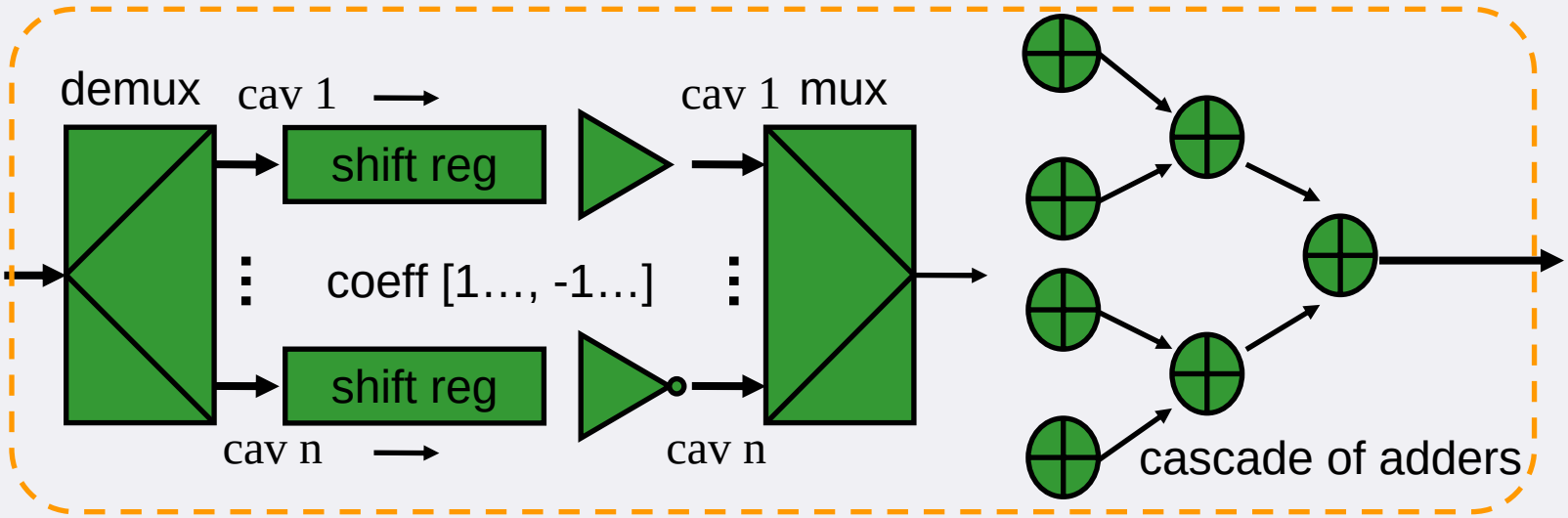
detn1 detn2



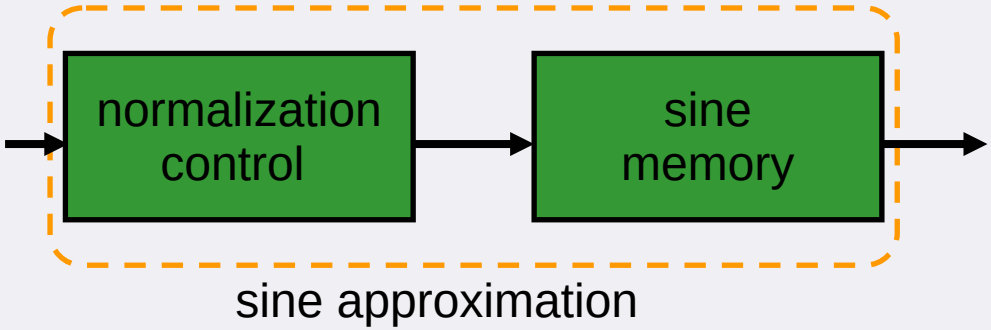
Implementation Structure



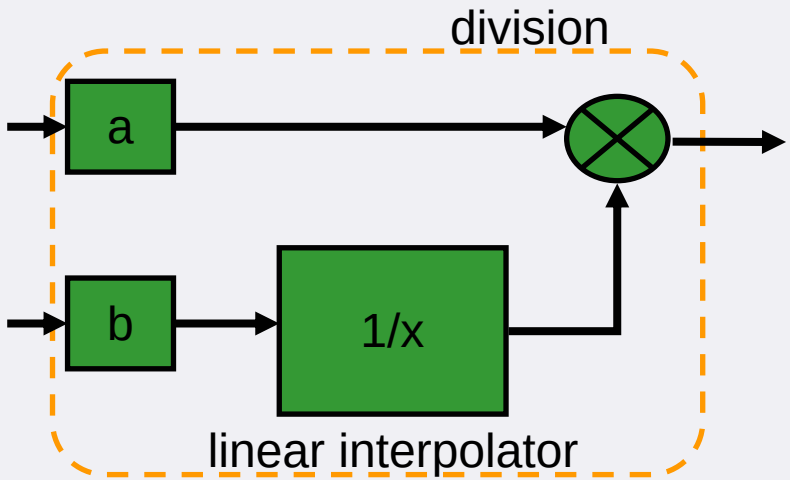
Block Diagram of Various Alg. Stages



derivative computation



sine approximation



linear interpolator

FPGA Resource Usage

FPGA	xc2vp50	
Slices	15622	Algorithm latency:
Flip Flops	18731	46 cycles for 8 cavities
LUTs	20597	
BRAMs	6	
MULT18x18	15	

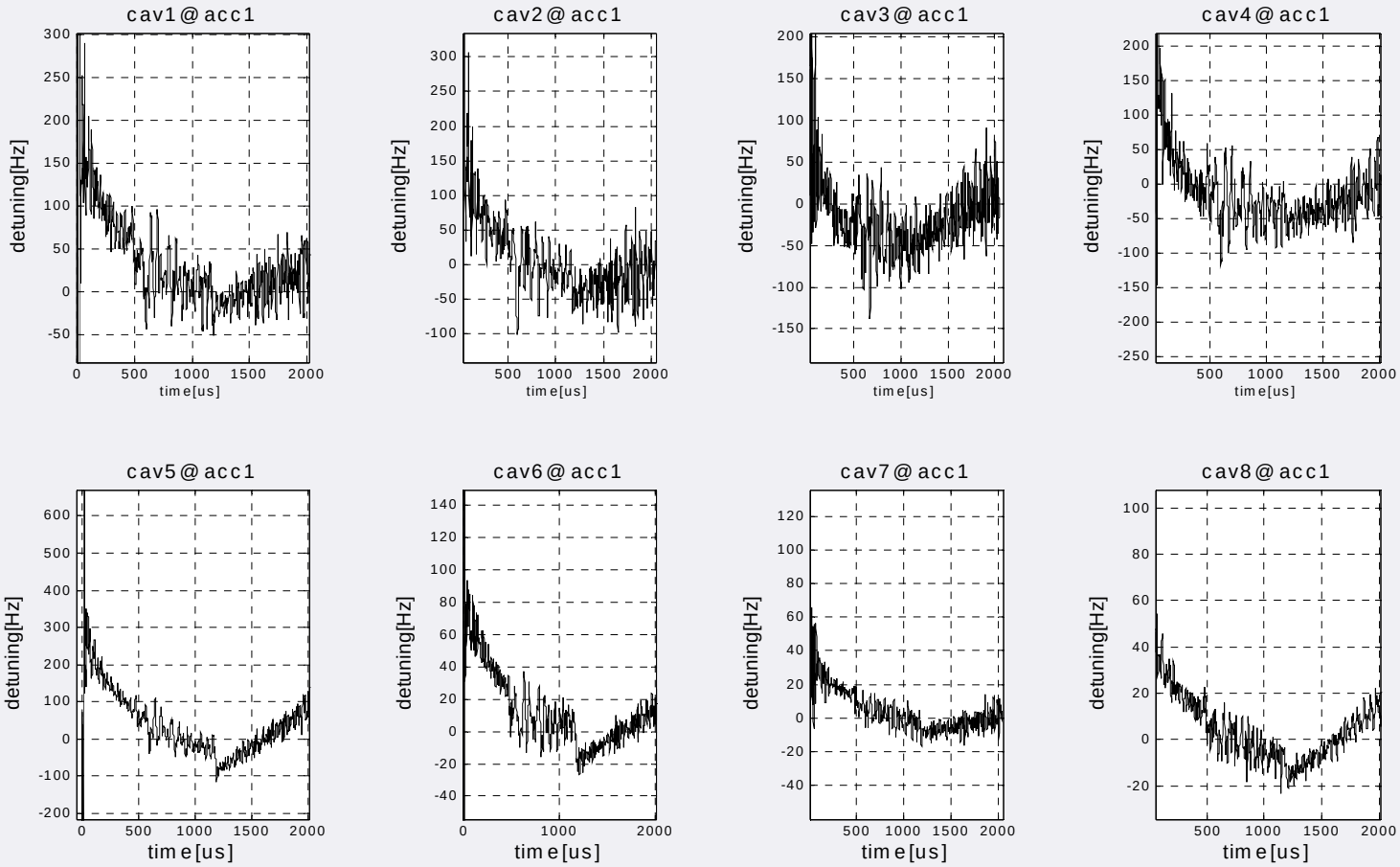
79% resources of FPGA chip (less then 50% goal)

timing compilation tests :
75 MHz passed
100 MHz passed

Detuning Tool Tests (ACC1)

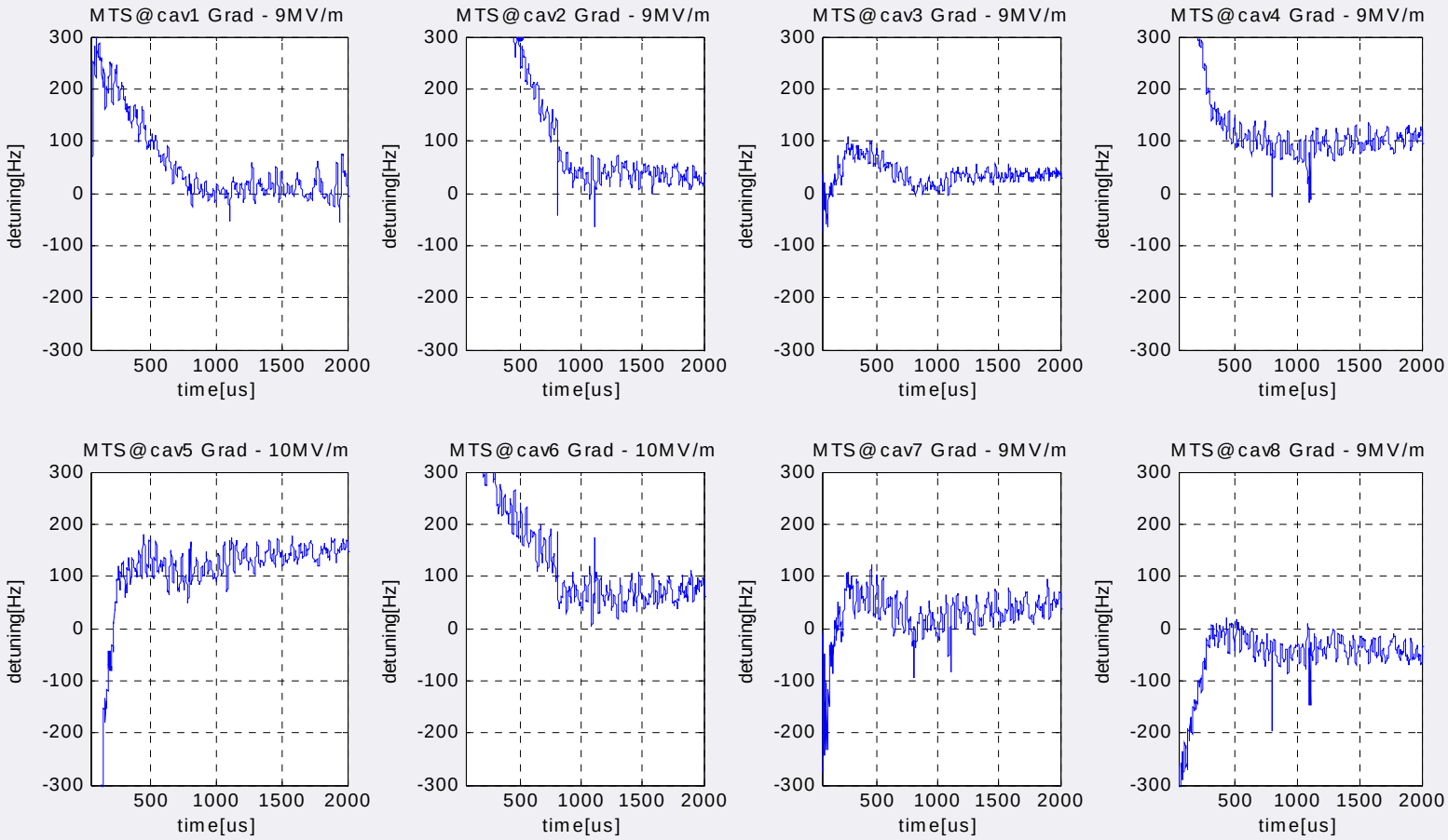
ACC1 – detuning computation in FPGA for 8 cavities simultaneously

– (SP Voltage 9 MV/m, T_{RF} = 5 Hz, RF pulse length – 500μs) - Jan 2008

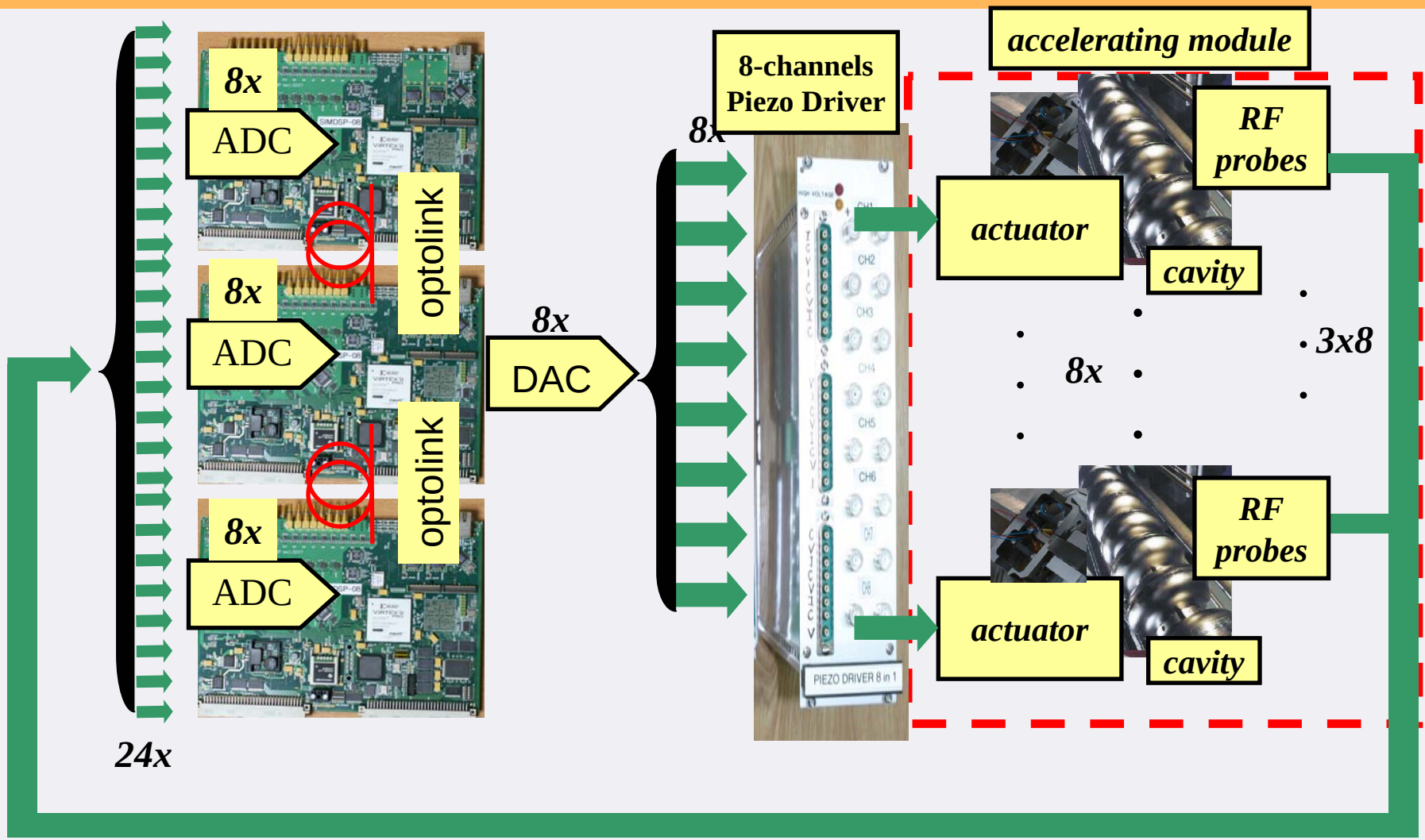


Detuning Tool Tests (MTS – modul 8)

MTS (module 8) – detuning computation in FPGA for 8 cavities simultaneously (SP Voltage 7 MV/m, T_{RF} = 5 Hz, RF pulse length – 300μs) - March 2008



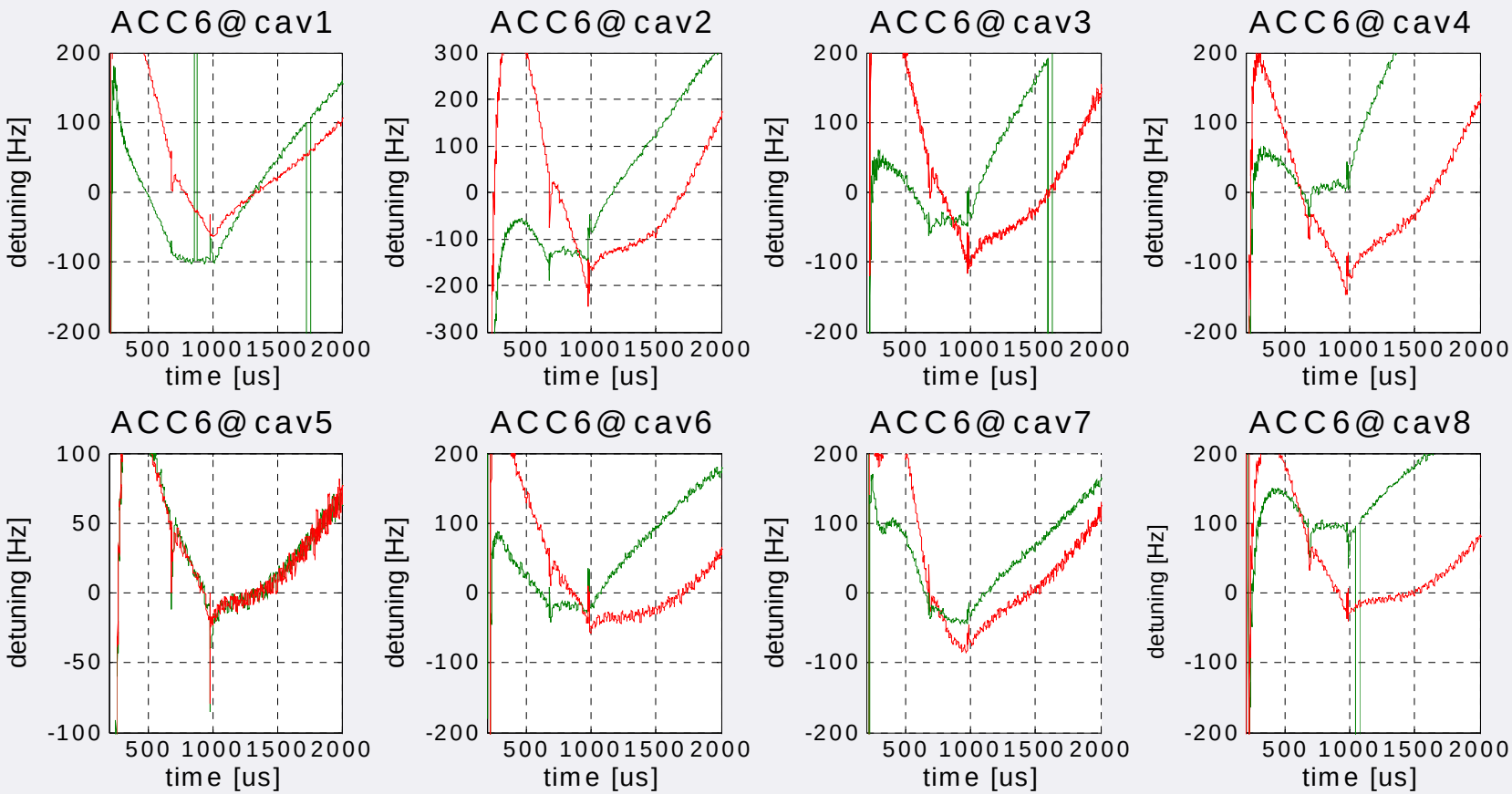
Detuning Tool Tests (ACC6)



Detuning Tool Tests (ACC6)

ACC6 – detuning computation in FPGA for 8 cavities simultaneously

– (SP Voltage 14 MV/m, T_{RF} = 5 Hz, RF pulse length – 300μs) - May 2008



Conclusions & Future Plans

Conclusions :

- Detuning measurement tool for multi-cavity configuration implemented in FPGA (SimconDSP controller),
- Online detuning measurements performed for ACC1, MTS (module 8) and ACC6
- Piezo Control System development (manuall operation for ACC6)

Future plans:

- Detuning measurement tool will be applied for automatic operation of Piezo Control System
- The computation algorithms will be ported to ATCA system for diagnostic
- Online detuning measurements will be used for microphonics identification

Thank You
For Your Attention