

# New features of the LLRF controller

Wojciech Jałmużna



# Agenda

1. Purpose of the presentation
2. Current status
3. Test system
4. Structure of the controller
5. Technical parameters
6. Results
7. Future plans



# Purpose of the presentation

The purpose of this presentation is:

- to show current status of the FPGA based controller for FLASH
- to summarize test results gathered during study weeks



# Current status of the project

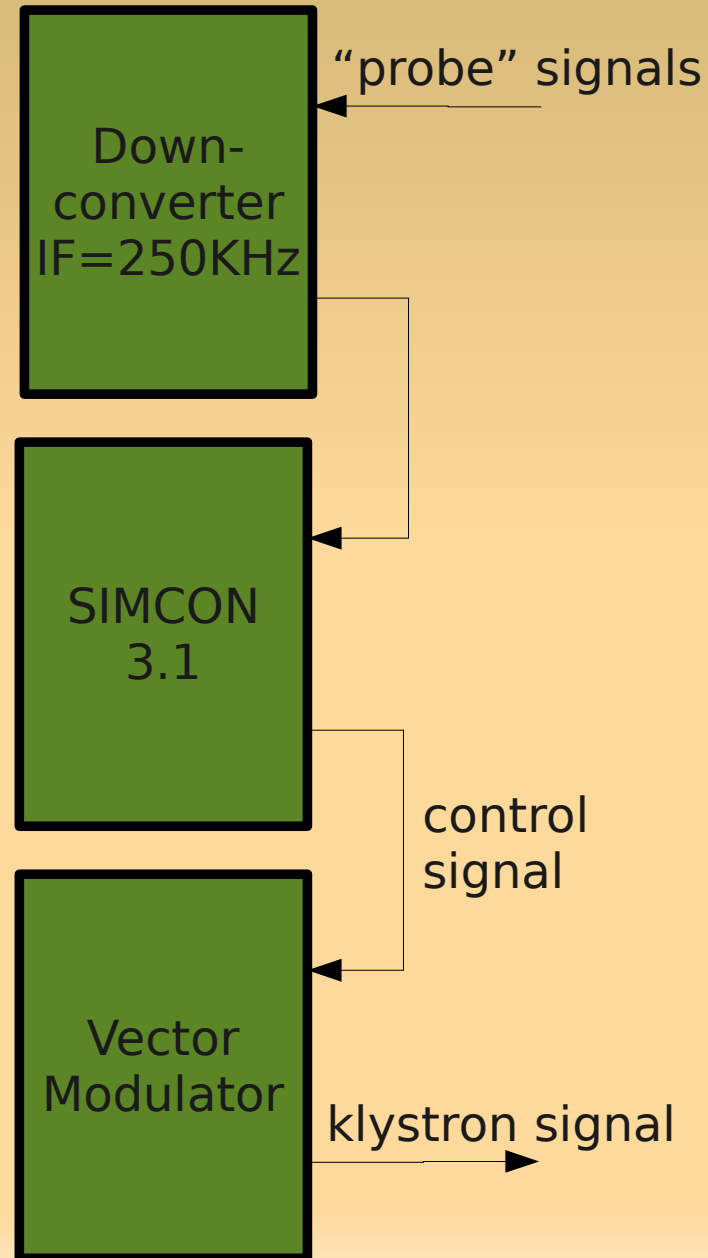
FPGA based controller  
permanently installed in ACC1.

Distributed architecture of the controller was  
proposed and implemented. It was tested for 24  
channels using ACC456.

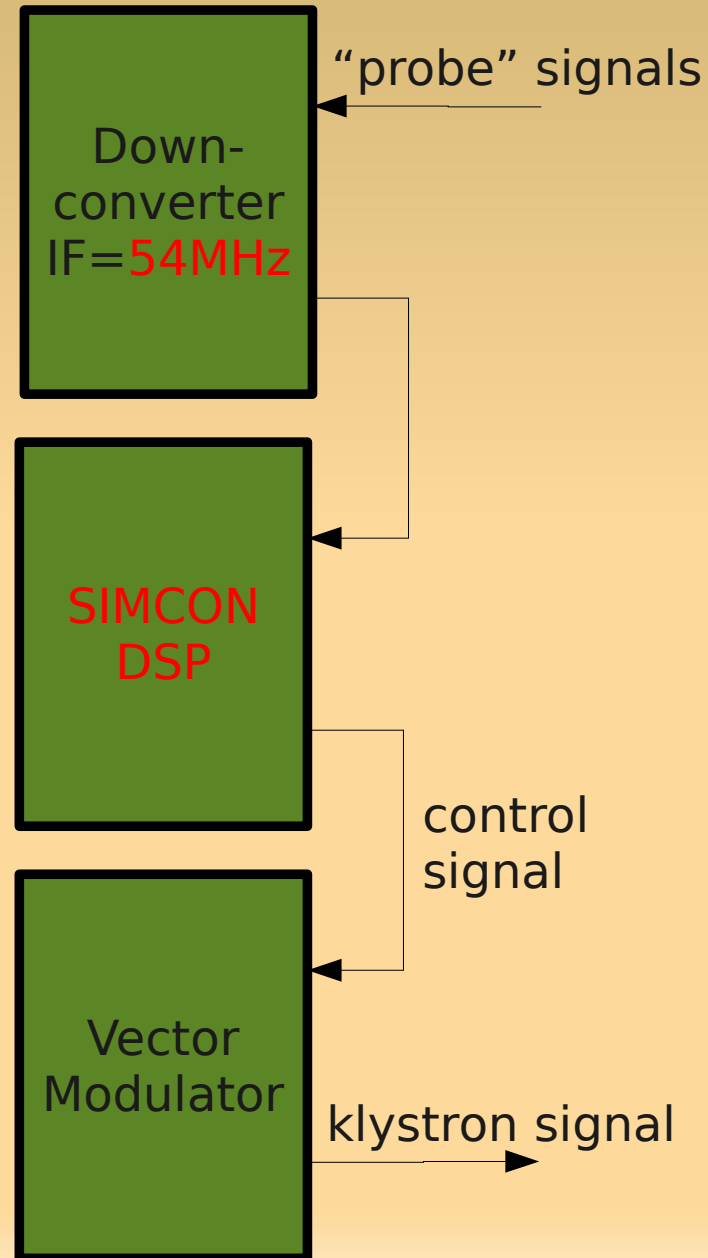


# Test system

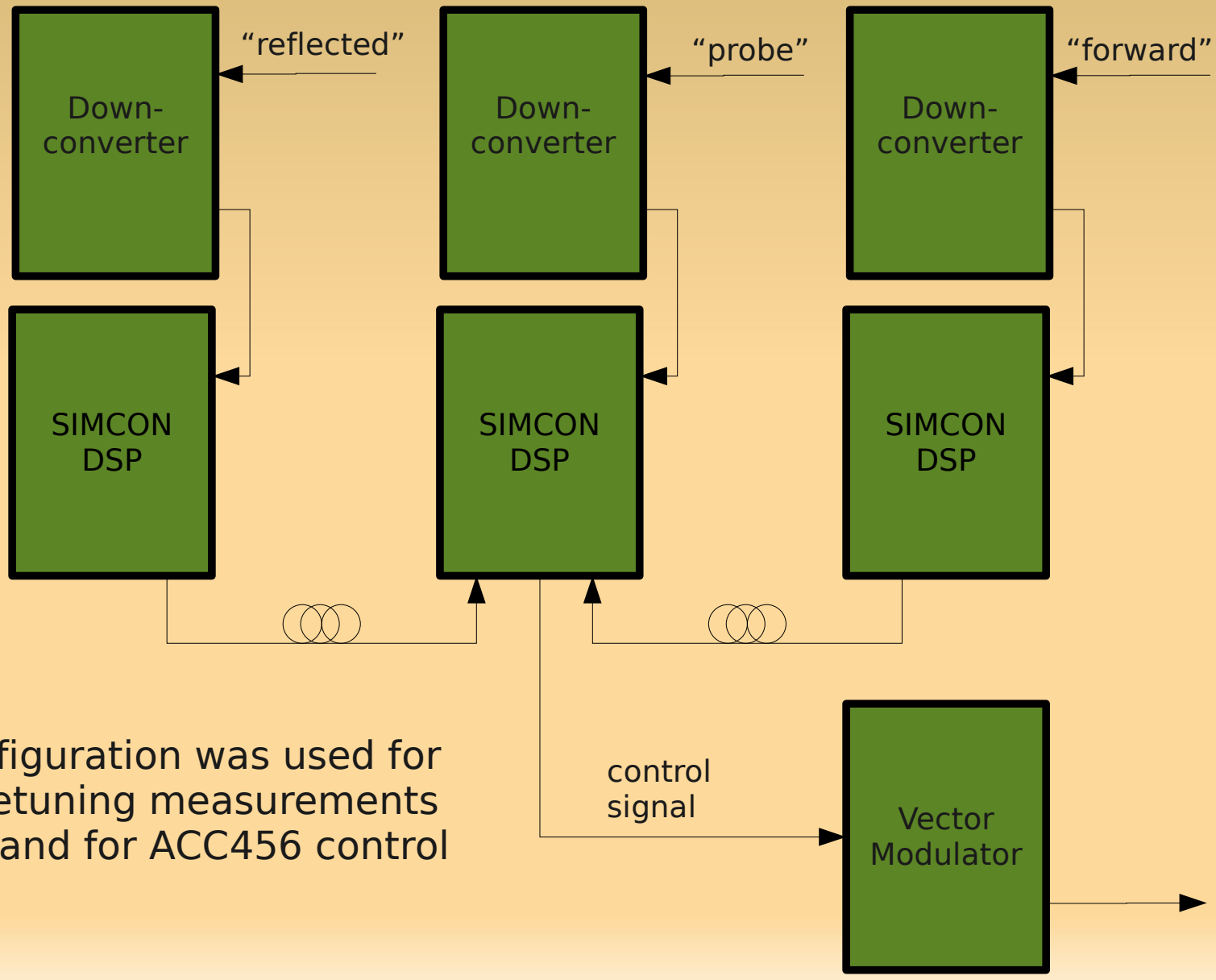
*Existing system*



# Test system

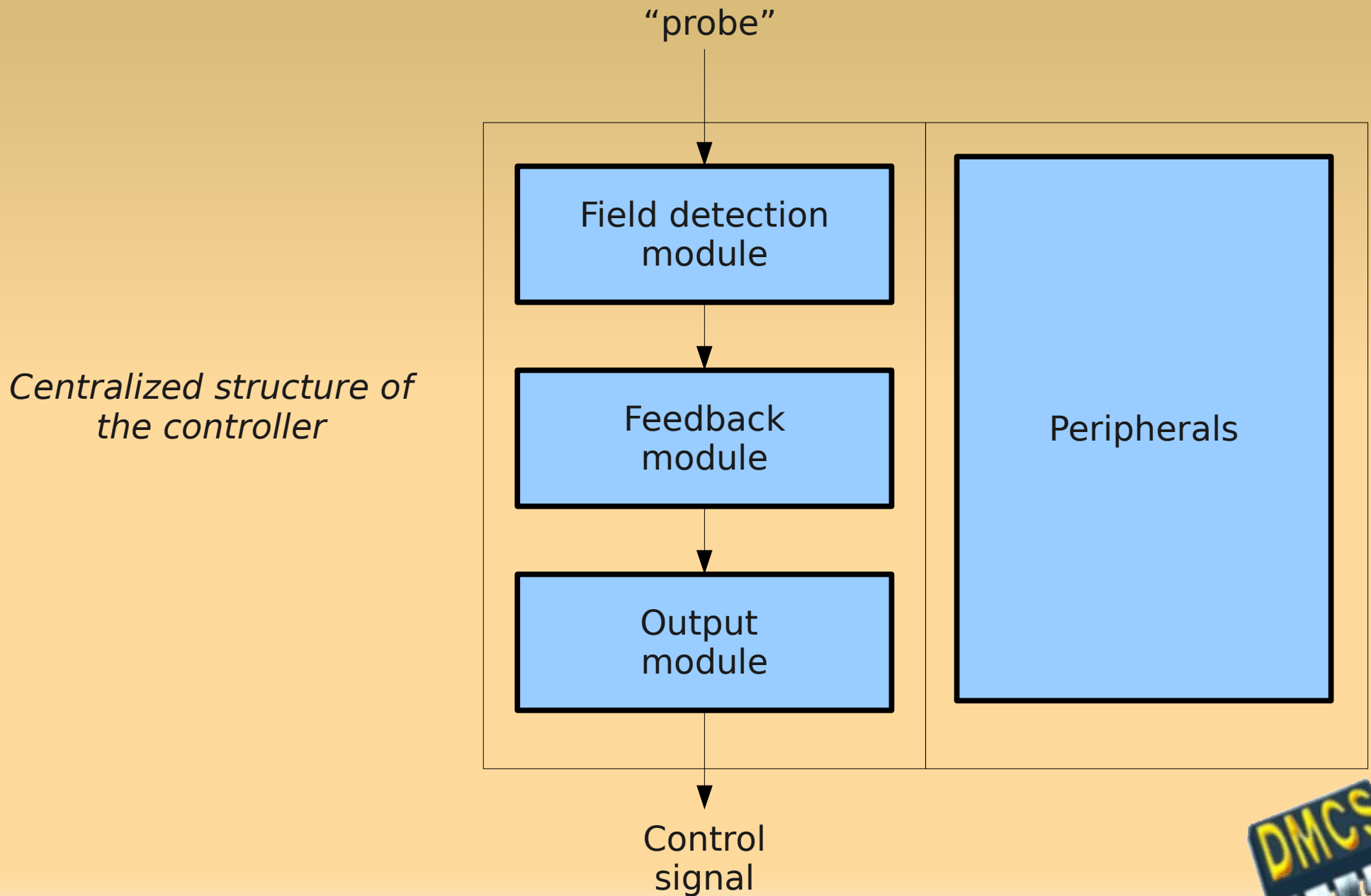


# Test system



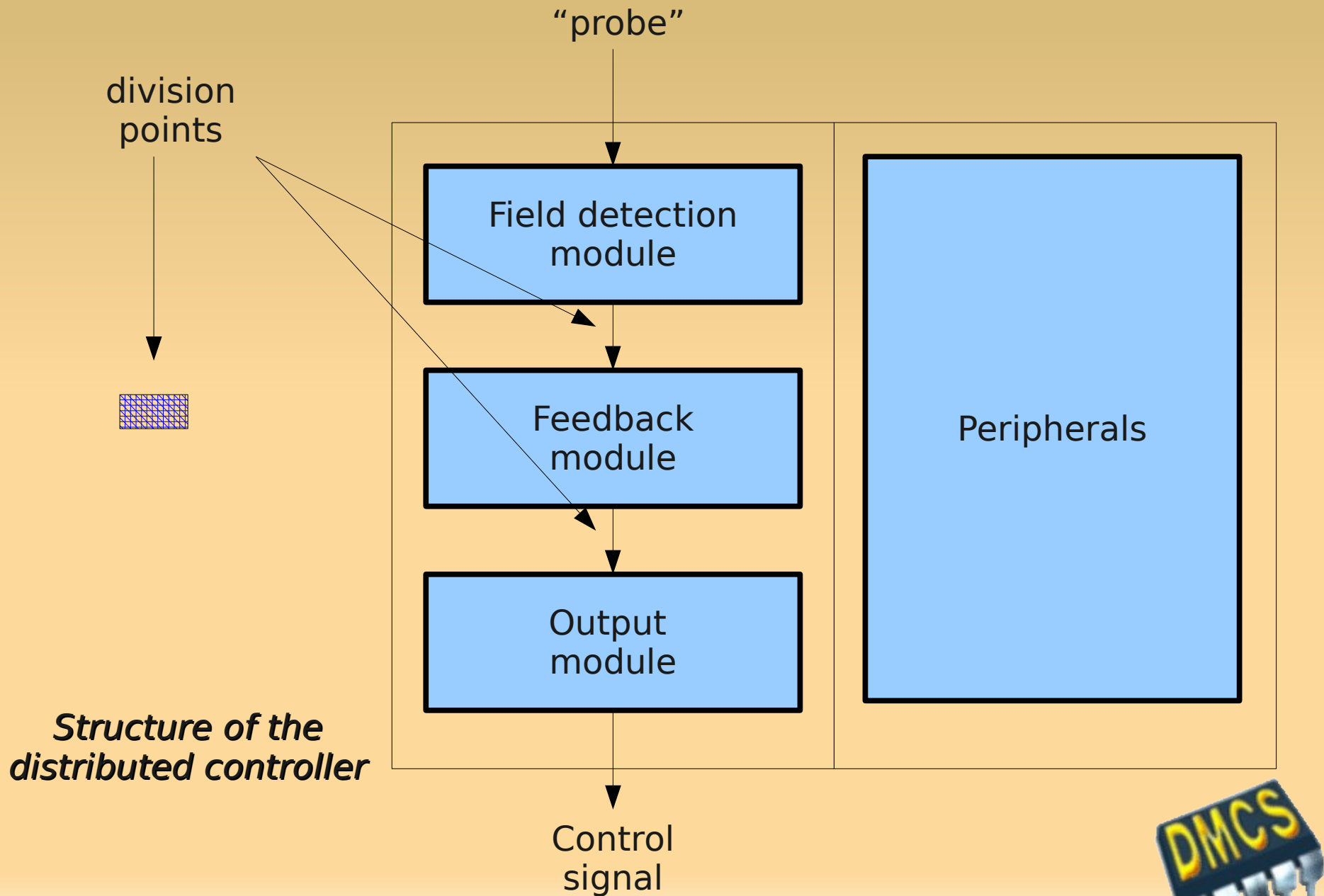
This configuration was used for online detuning measurements in ACC1 and for ACC456 control

# Structure of the controller

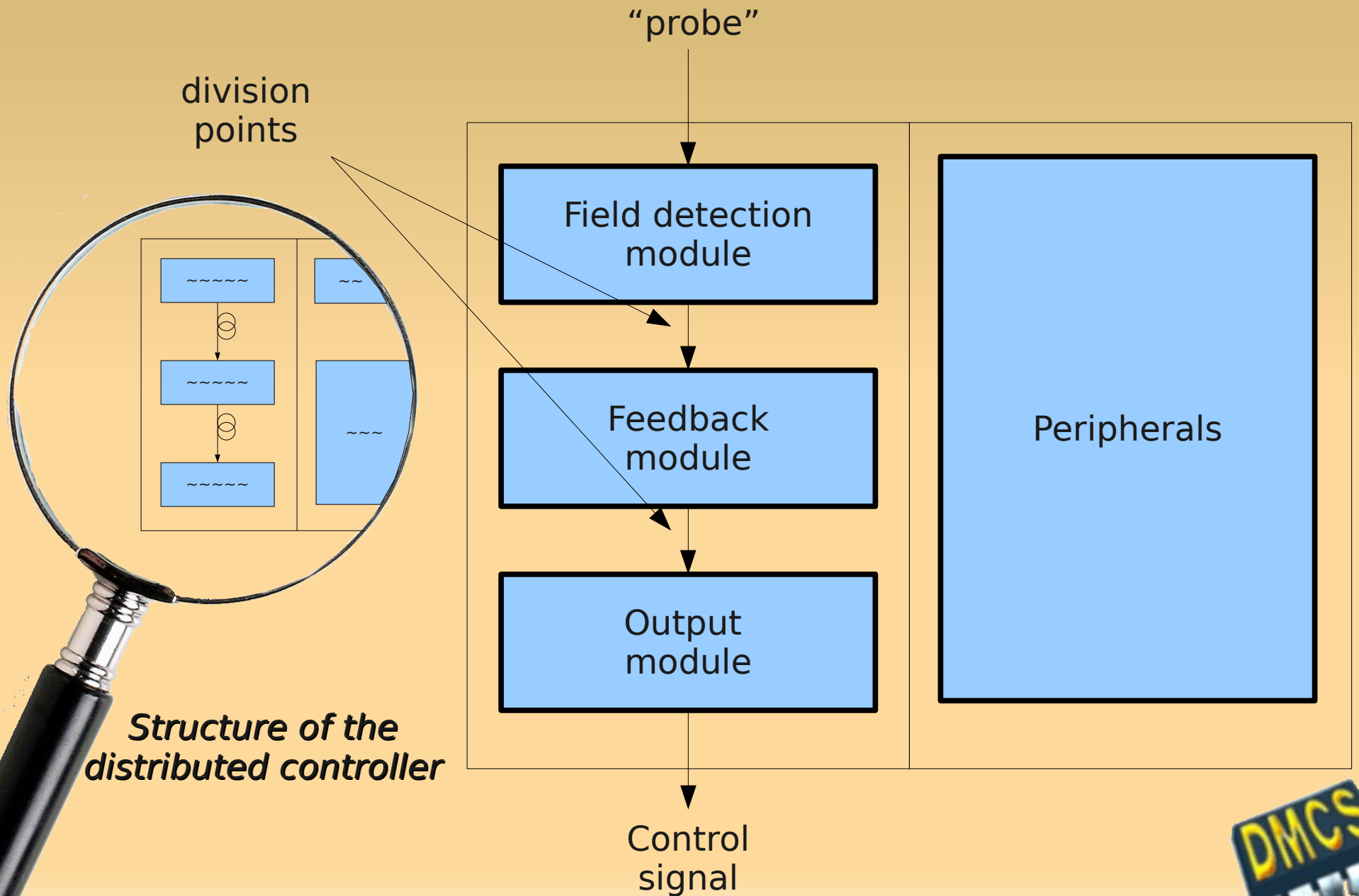




# Structure of the controller



# Structure of the controller



*Structure of the distributed controller*



# Technical parameters

1. Numerical precision: 18 bits
2. Operating frequency: 100 MHz
3. Resource usage: up to 60% for Virtex 2 Pro 30
4. Tools used: Xilinx ISE package



# ACC1 controller

What is currently installed in ACC1 ?

Basic version of the controller with beam load compensation feature together with klystron linearization module.

Tomorrow we will install and test AFF algorithm.

# Modes of operation

There are two modes of operation

1. Diagnostic mode
2. Operational mode

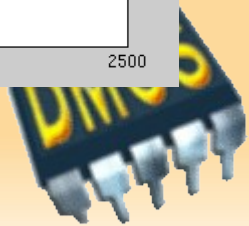
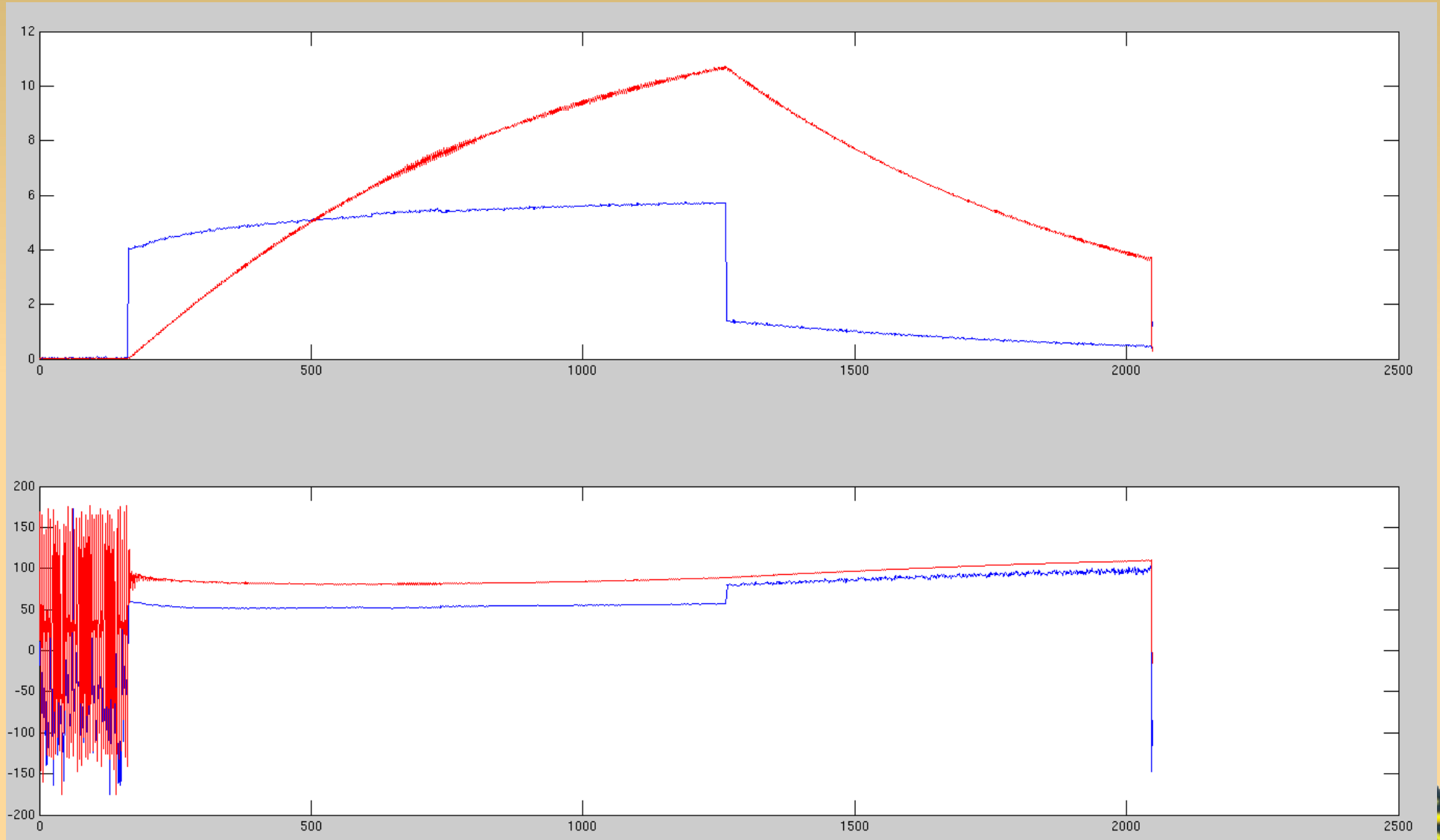


# SEL results

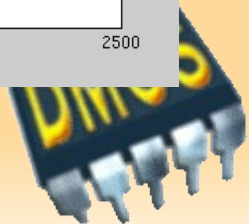
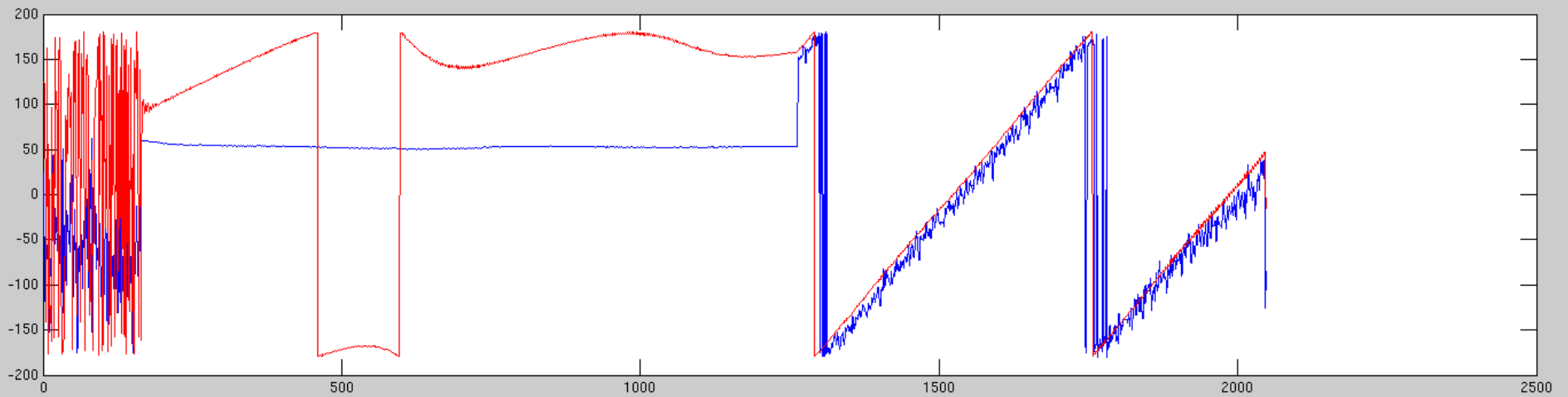
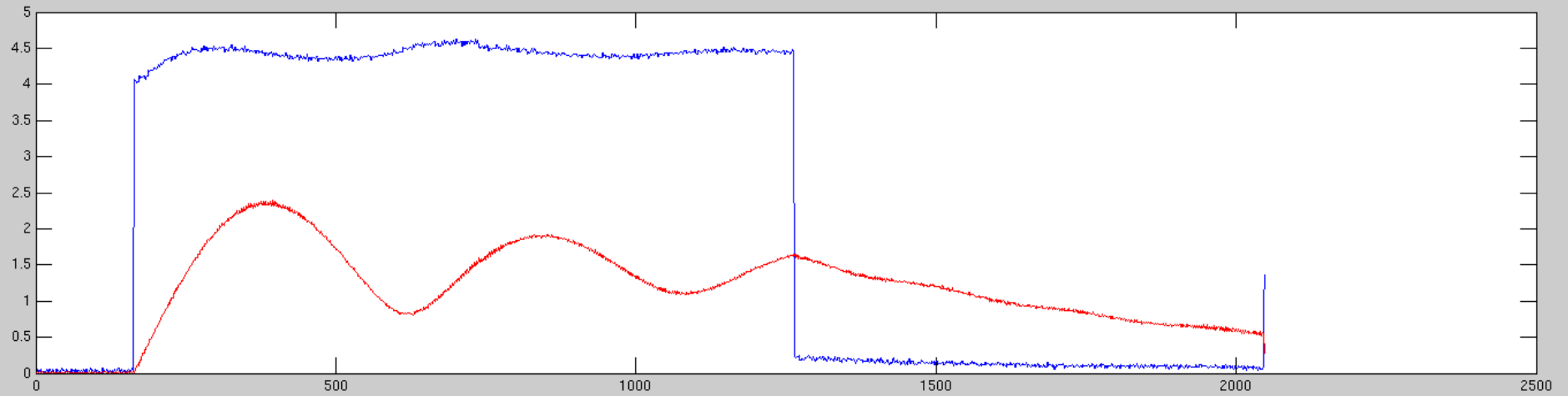
Self excited loop makes it possible to fill the cavity which is detuned from its resonance frequency even by a large offset.

Currently it is possible to work in SEL mode using amplitude limiter on the output of the controller

# SEL results (1)

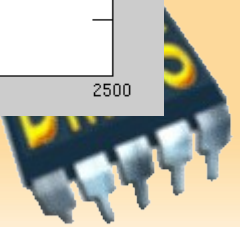
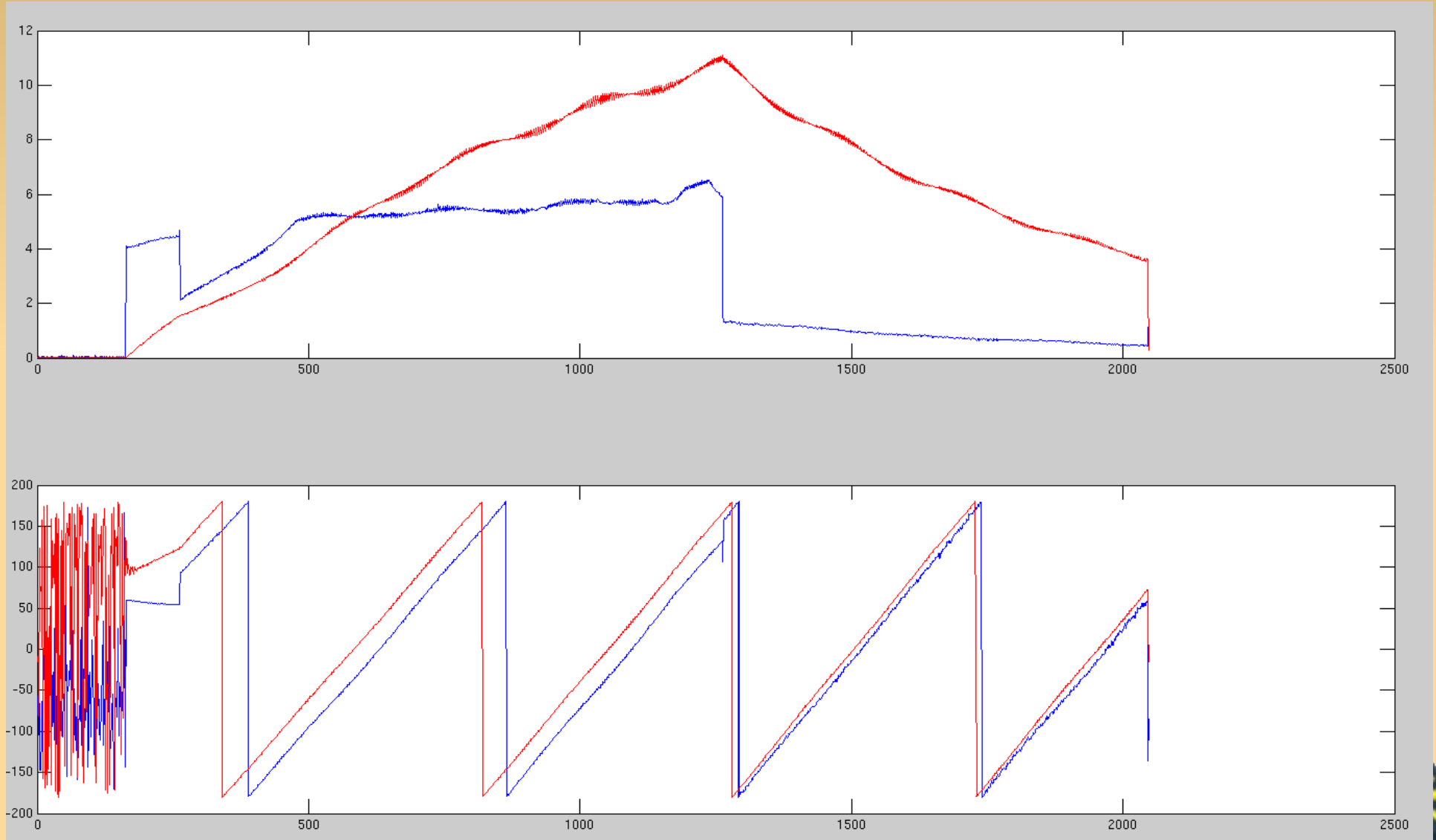


# SEL results (2)

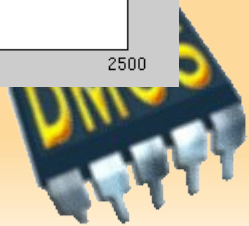
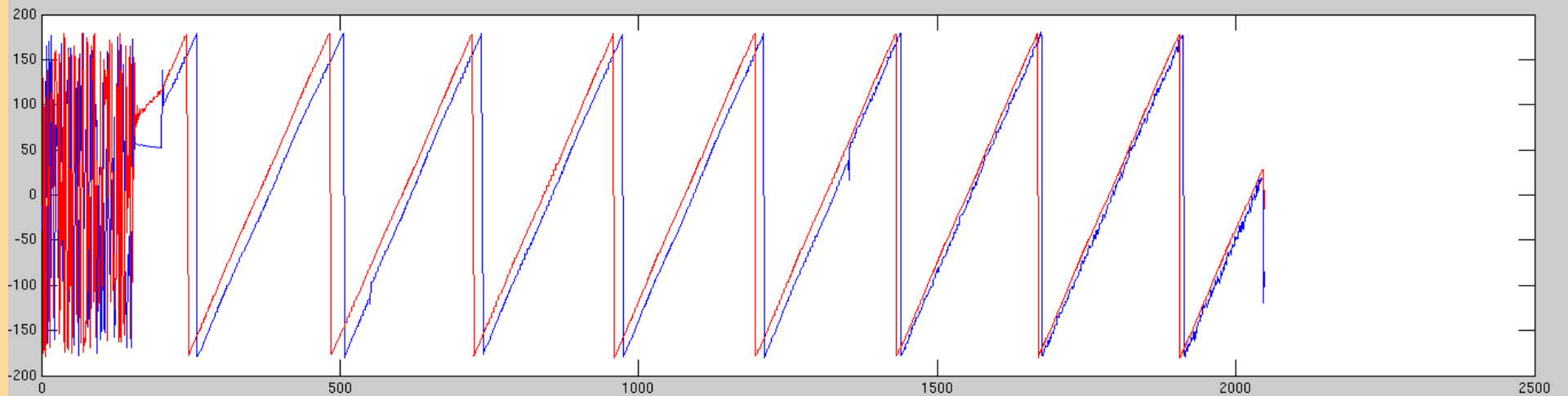
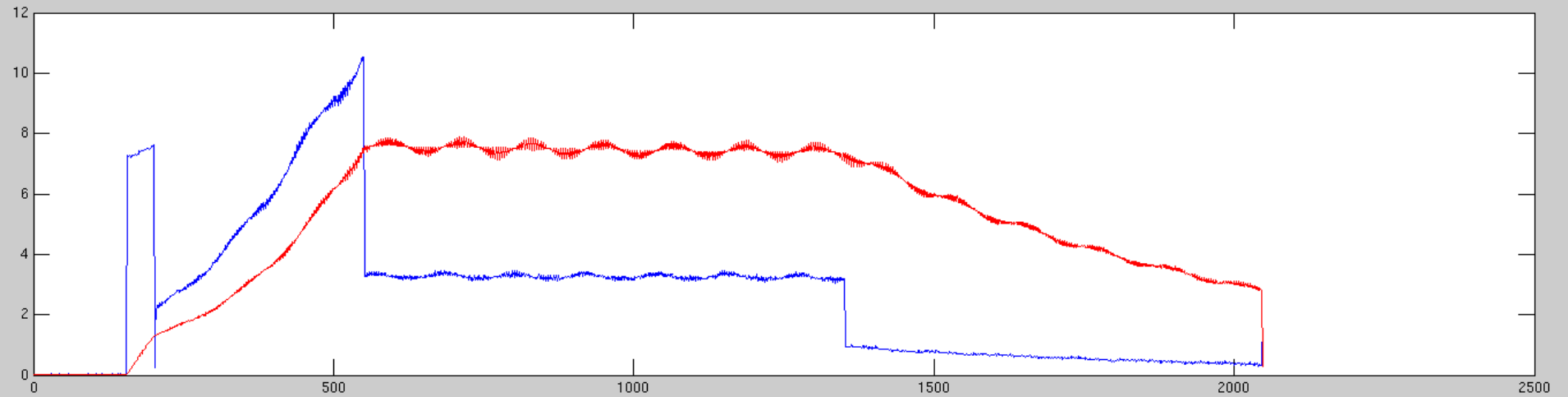




# SEL results (3)



# SEL results (4)

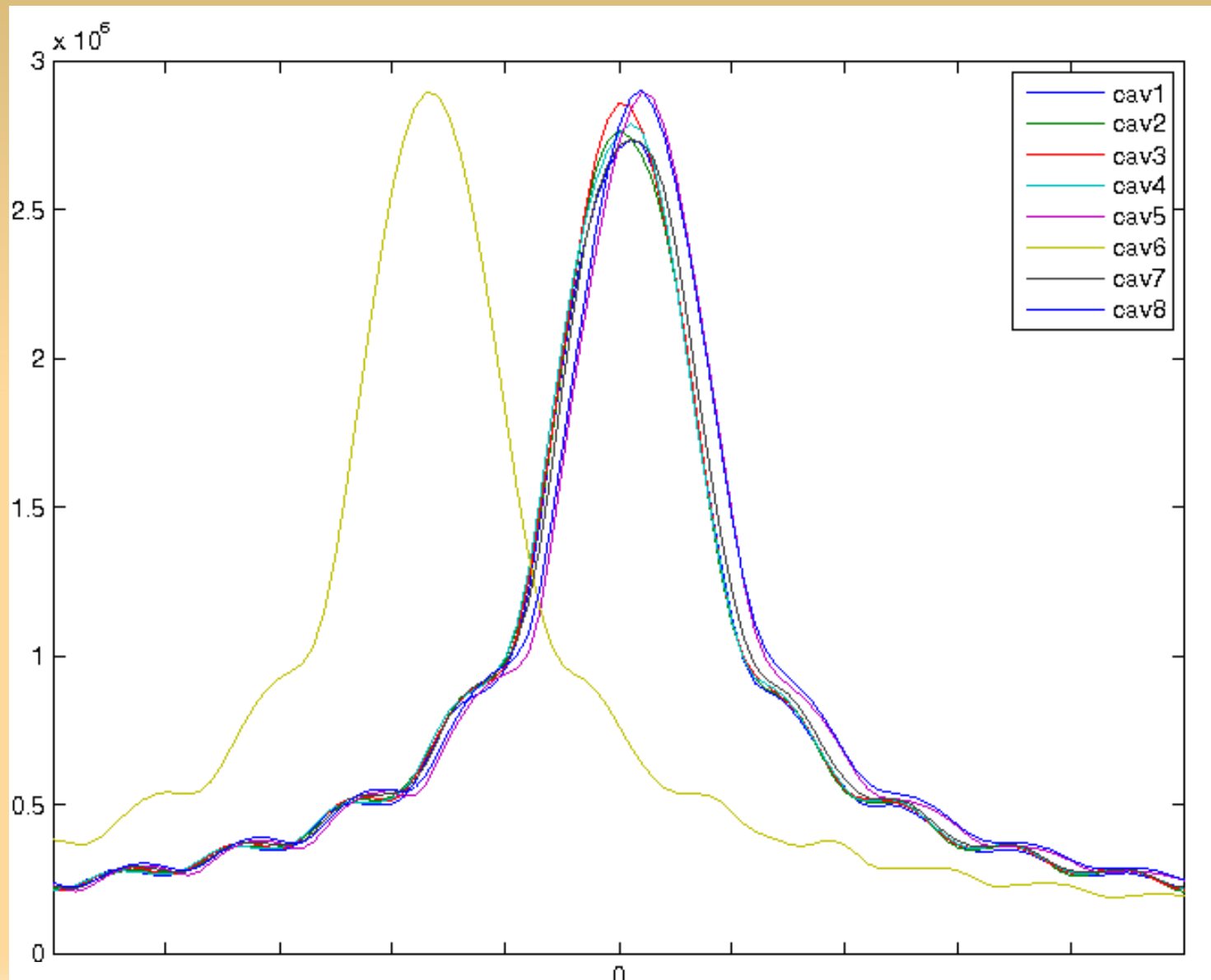


# Frequency Sweep Mode

This function measures the frequency response of the individual cavities using constant amplitude and slope on the phase of the control signal .

The final implementation will work with increased frequency of output update rate to get more precise frequency control.

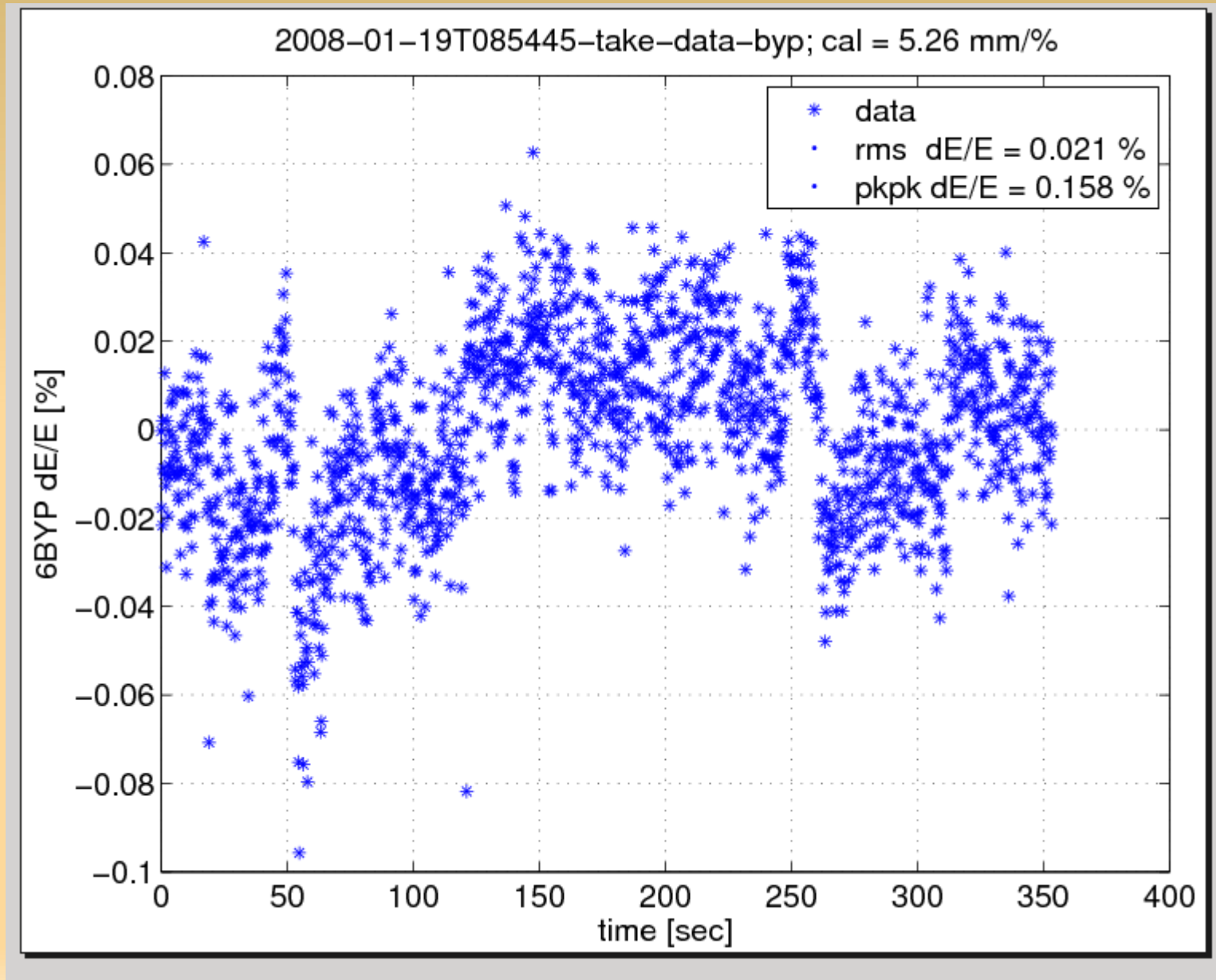
# Frequency Sweep Mode



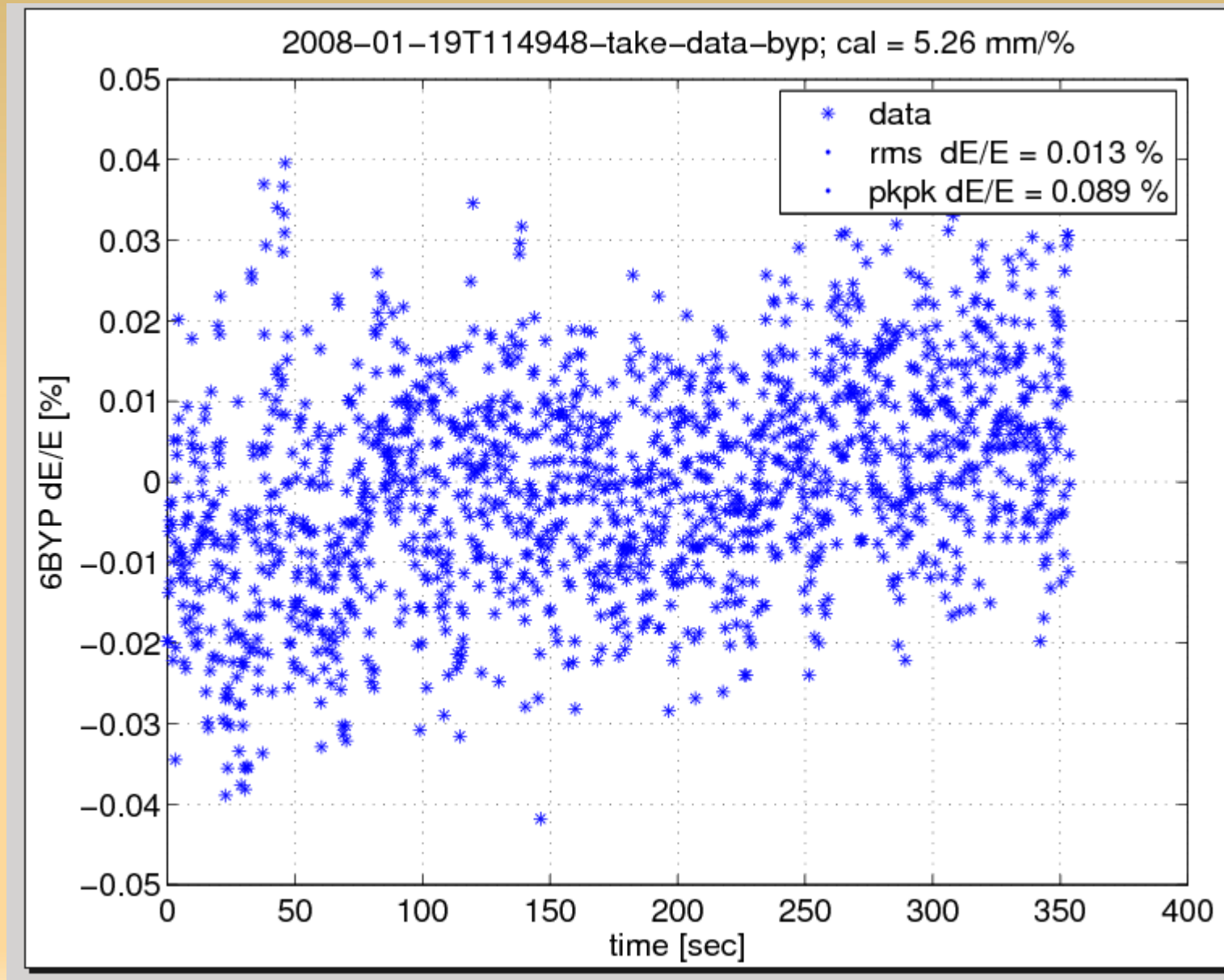
# Beam stability – ACC456 (1)

The distributed version of the controller was used to drive ACC456 modules. To compare the quality of the control between DSP and FPGA based systems beam energy stability measurements have been performed.

# Beam stability – ACC456 (1)



# Beam stability – ACC456 (2)



# AFF tests

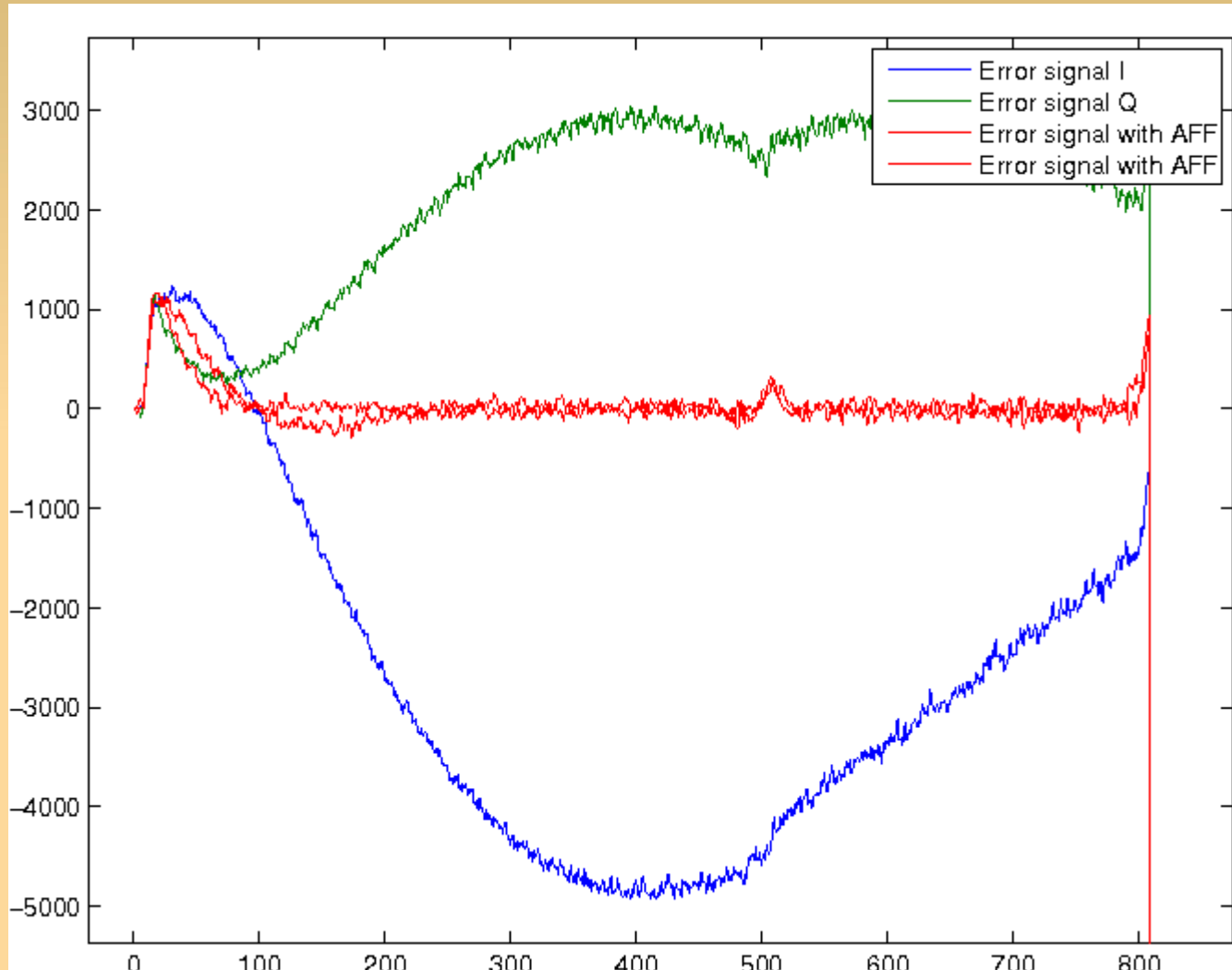
Algorithm proposed by A. Brandt was implemented for FPGA based controller. Currently there are 3 possible ways to run it:

- Matlab implementation
- FPGA implementation
- Embedded system implementation

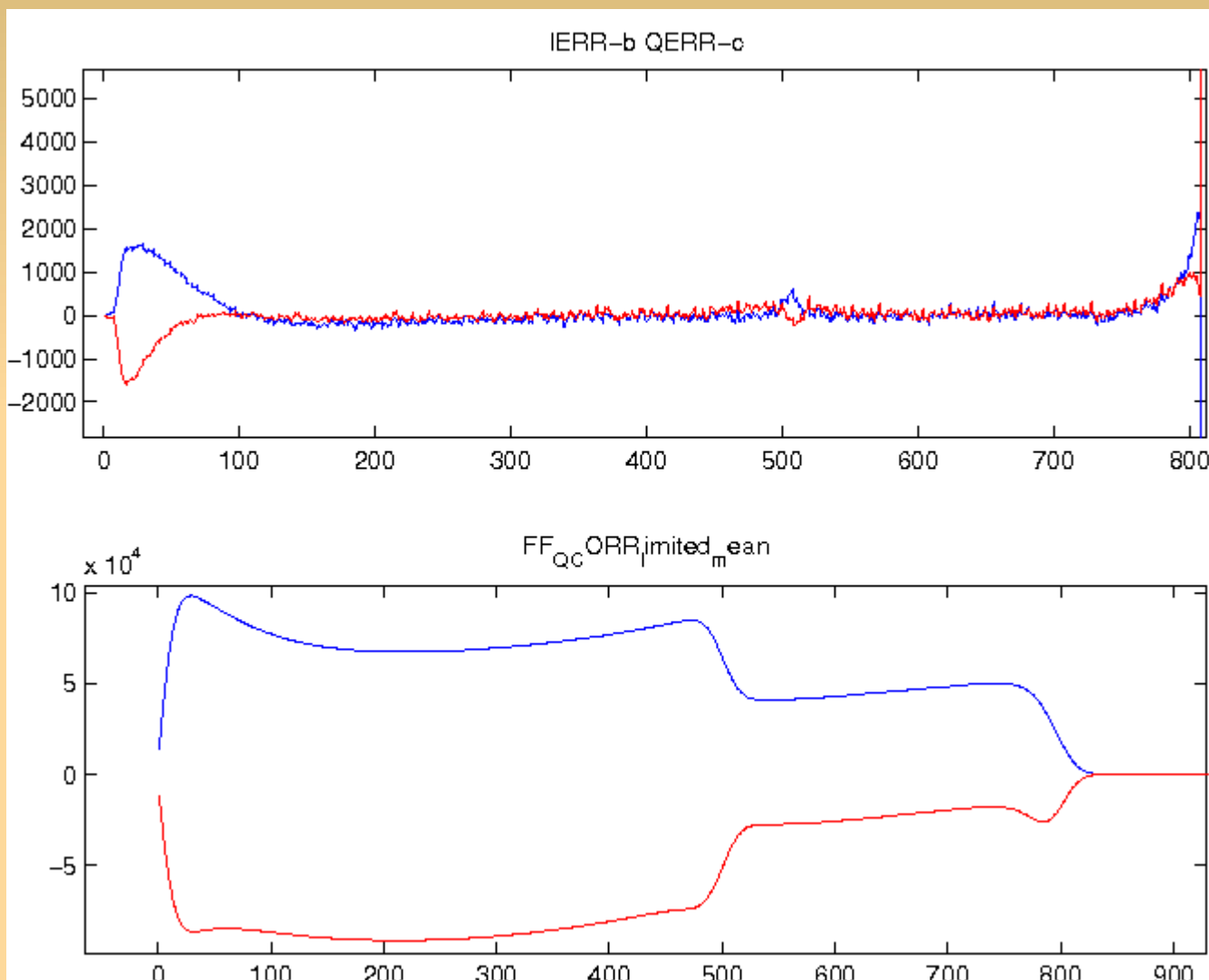
In near future there will be DSP implementation as well



# AFF tests (1)



# AFF test (2)



# Additional results

1. Amplitude-Q control
2. Klystron linearization component
3. Control using  $IF = 54\text{MHz}$
4. Beam energy stability after ACC1 with tuned parameters
5. Delay scans



# Future plans

1. To measure the performance of the controller in ACC23 modules
2. To fully integrate controller with DSP processor on SIMCON DSP board
3. Run the whole machine using FPGA boards and evaluate performance



Thank you for your attention